P5E-VM DO

R1.02G
2007_0824_1516

2007.08.24

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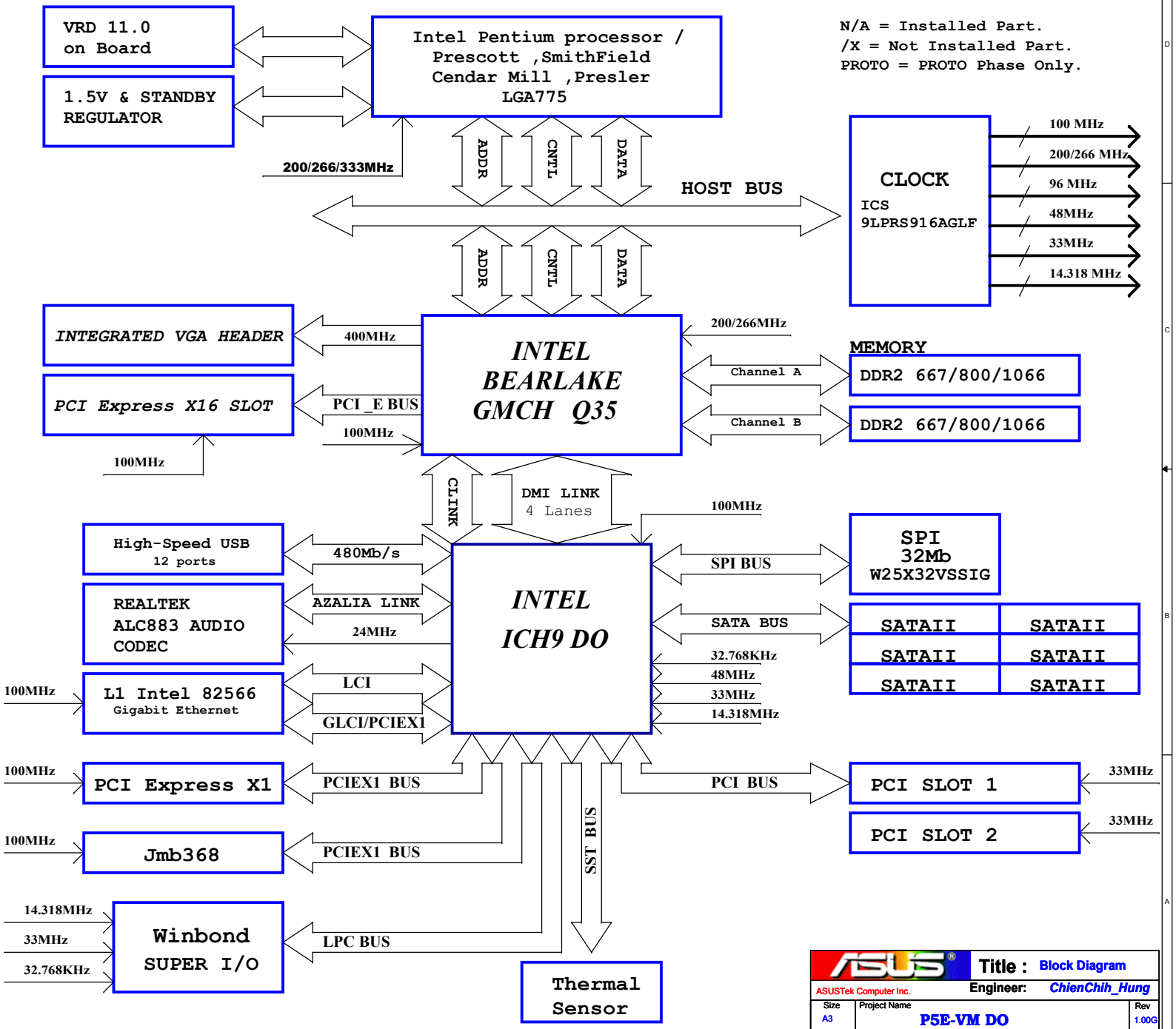
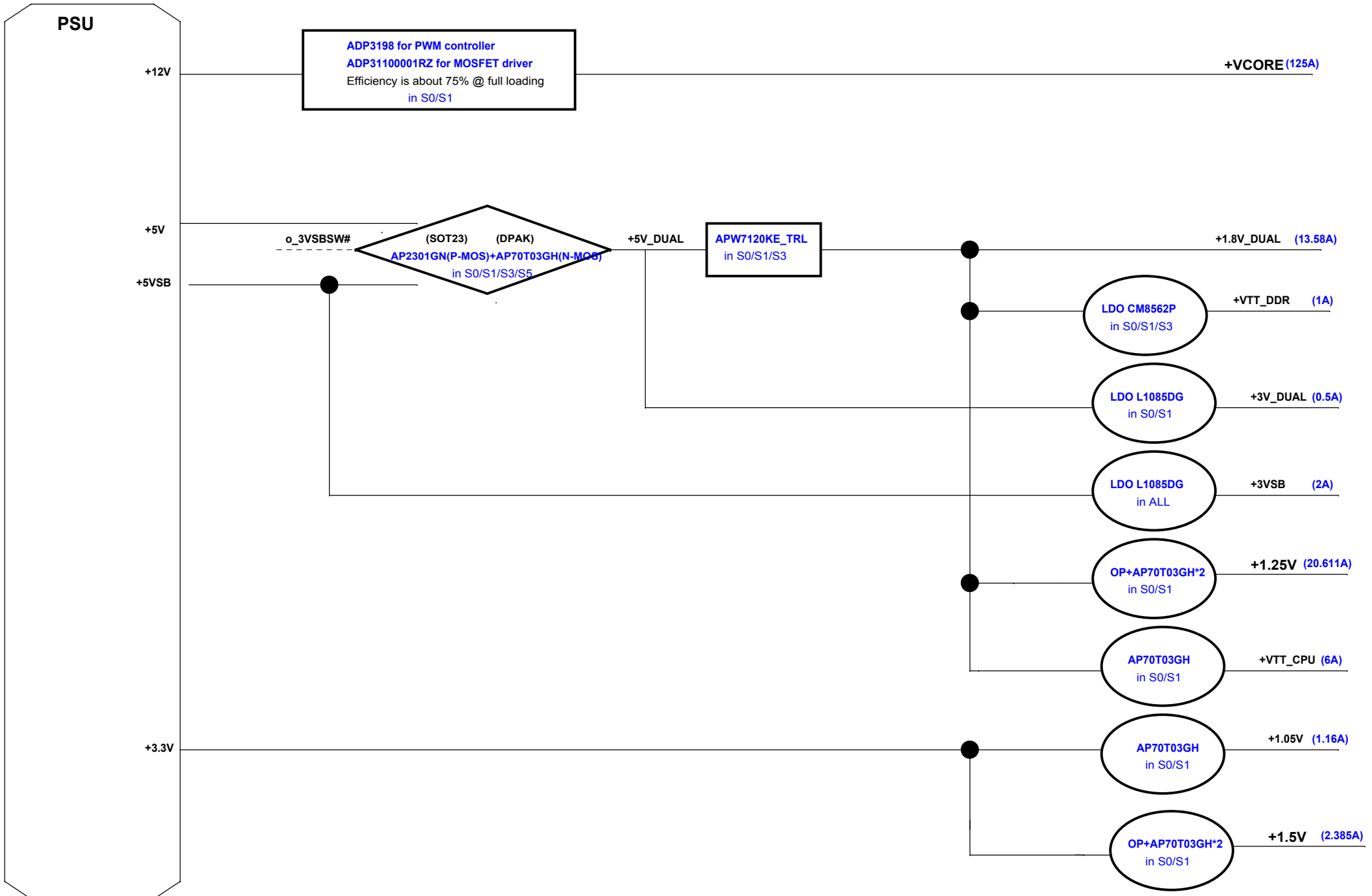
58	POWER CONNECTOR
59	PANEL & HotStart
60	VCORE CONTROLLOR
61	VCORE DRIVERS
62	+5V_DUAL& +3VSB&+3V_DUAL
63	+1.5V
64	+1.8V_DUAL& VTT_DDR
65	+1.25VDUAL & +1.05V &+VTTCPU
66	+1.25V
67	NOS(Intel)
68	Screw Hole
69	EMI
70	Change PCB version List

CAD Note:
Default component footprint is SMD 0402 type. Difference footprint show on schematics.

N/A = Installed Part.
/X = Not Installed Part.
PROTO = PROTO Phase Only.



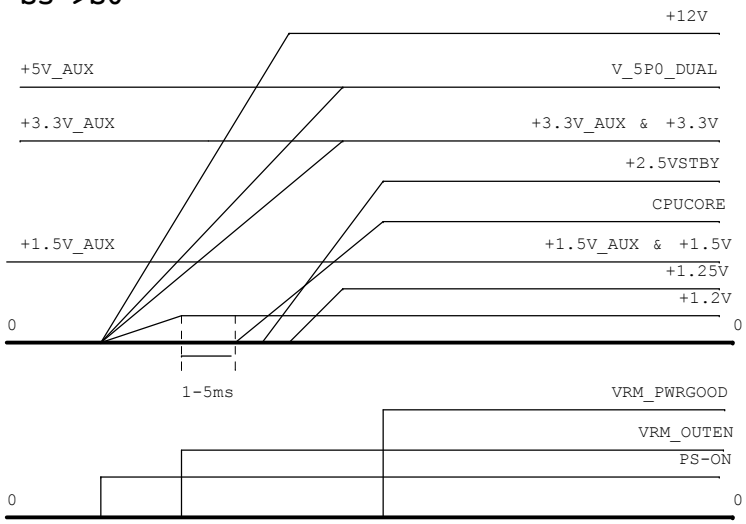
ASUSTek Computer Inc.	Title : Block Diagram	
	Engineer: ChienChih_Hung	
Size: A3	Project Name: P5E-VM DO	Rev: 1.00G
Date: Tuesday, November 13, 2007	Sheet 1 of 70	



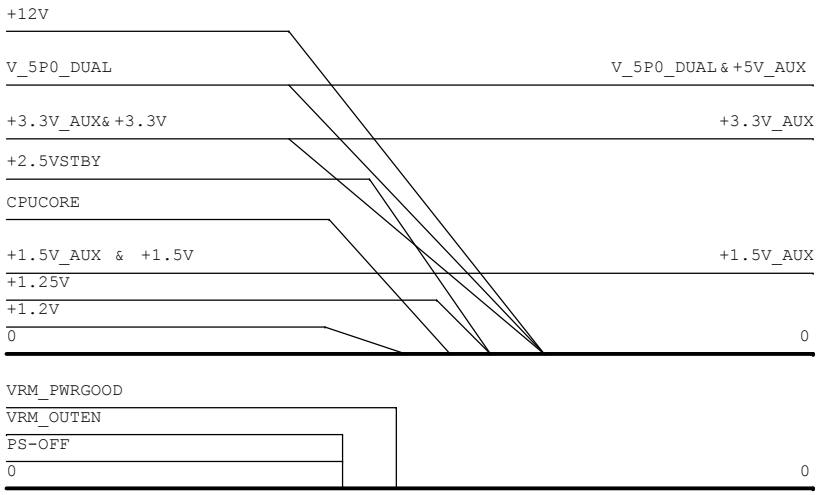
P5B-BVM DO

ASUSTek Computer Inc.	Title : Power Flow	
	Engineer: Barry_Sue	
Size: A3	Project Name: P5E-VM DO	Rev: 1.00G
Date: Friday, March 28, 2008	Sheet 2 of 70	

S5->S0

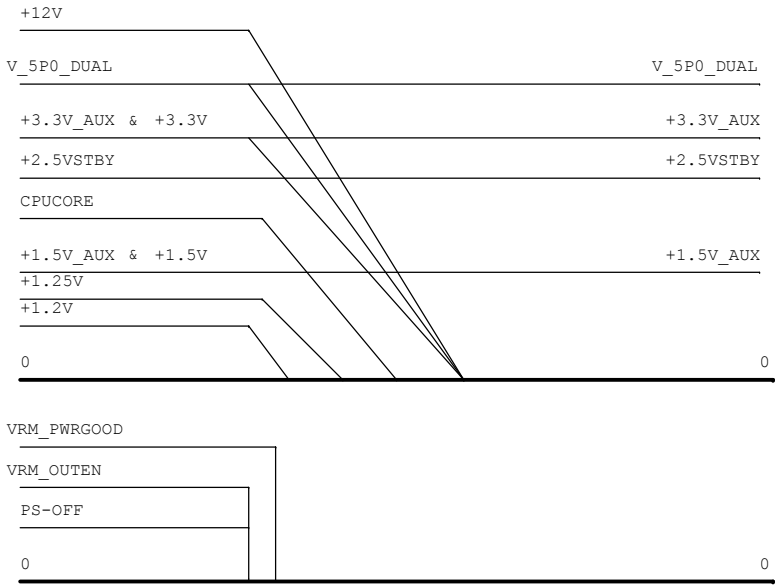


S0->S5

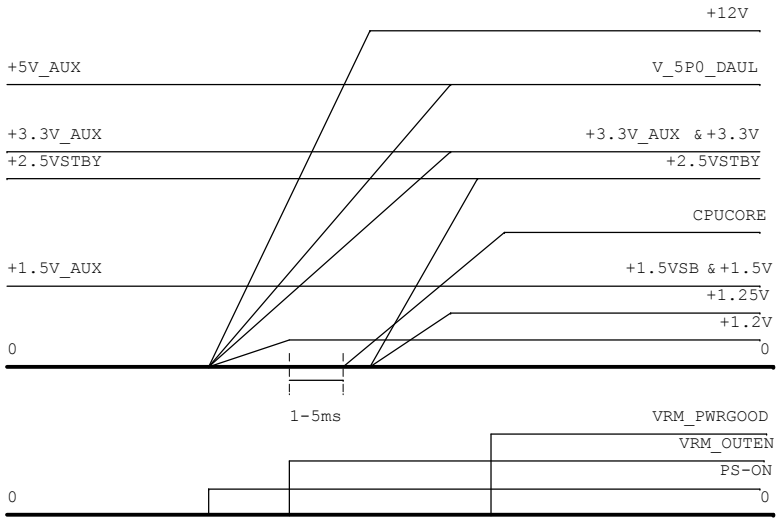


1.CPUCORE must rise after the voltage across 90% of +1.2V,andthe interval is within 1-5ms
2.VRM_OUTEN rises after the voltage across 90% of its specified value

S0->S3



S3->S0



1.CPUCORE must rise after the voltage across 90% of +1.2V,andthe interval is within 1-5ms
2.VRM_OUTEN rises after the voltage across 90% of its specified value

S0: Windows Running +12V,V_5P0_DUAL,+3.3V,+3.3V_AUX,+2.5VSTBY,CPUCORE,+1.5V,+1.5V_AUX,+1.25V,+1.2V existed
S3: Windows Standby V_5P0_DUAL,+3.3V_AUX,+1.5V_AUX,+2.5VSTBY existed
S5: AC Power On Only +5V_AUX,+3.3V_AUX,+1.5V_AUX existed

<Variant Name>

ASUSTek Computer Inc.

Title : Power Sequence
Engineer: Tyler_Yuan

Size	Project Name	Rev
A3	P5E-VM DO	1.01G

Date: Friday, March 28, 2008 Sheet 3 of 70

Prescott,Smithdield, Presler & Conroe

VCORE	125A 130W
+1.2V_FSB_VTT	5.3A 6.36W

CK505

+1.8VSB	80mA
+3VSB	250mA

Bear lake

+1.5_DUAL	3.33A (S0,S1)
+1.5_DUAL	350mA (S3&SMCLK)
+1.2V_FSB	VTT 1.2A
+1.25V	13.8A
	2.47A (DMI&PCIE)
	4.9A (CL)
+3V	66mA (DAC)
	15.8mA (CMOS)

ICH9

+1.2V_FSB_VTT	2mA
+1.5V	1.652A (USB&SATA&PLL)
	646mA (PCIE)
	15mA 0.0225W(CL internal)
	74mA 0.111W(LAN)
+1.25V	41mA (DMI)
+1.05V	1.43A(Core)
	37mA (CL internal)
	157mA 0.165W(10/100 LAN internal)
+3VSB	19mA (CL)
	32mA (HDA S3,S4&S5)
+3V	1mA(GbE-LAN)
	19mA (10/100 LAN)
	32mA (HDA S0&S1)
VCCRTC	308mA (VCC3_3)
	6uA

DDR2 DIMM

+1.8_DUAL	(S0,S1)
+1.8_DUAL	TBD(S3)
VTT_DDR	0.83A (S0)
	TBD (S3)

PCI EXPRESSx16

+12V	5.5A 66W
+3VSB	0.375A 1.24W (wake)
+3VSB	20mA 66mW (no wake)
+3V	3.0A 9.9W

PCI SLOT

+3VSB	0.375A 1.24W (wake)
+3VSB	20mA 66mW (no wake)
+3V	7.6A 25.08W
+5V	5A 25W
+12V	0.5A 6W
-12V	0.1A 1.2W

KB/MS

+BUSB	0.5A 2.5W

USB 12 PORT

BUSB+5V	2A(S0,S1)
BUSB+5V	15mA 75mW (S3)
FUSB+5V	4A (S0,S1)
FUSB+5V	10mA 50mW (S3)

SPI

+3VSB	30mA 99mW

FAN

+12V	0.5A 6W

ALC885 CODEC

+5VA	200mA 1W
+3V	40mA 132mW

Atheros L1

+3VSB	15.5mA 51.15mW (I/O&LED)
+2.5VSB	418.2mA 7.53W(Analog)
+1.5VSB	277.2mA 277.2mW (Core)

PCIEX1

+12V	5.5A 66W
+3VSB	0.375A 1.24W (wake)
+3VSB	20mA 66mW (no wake)
+3V	3.0A 9.9W

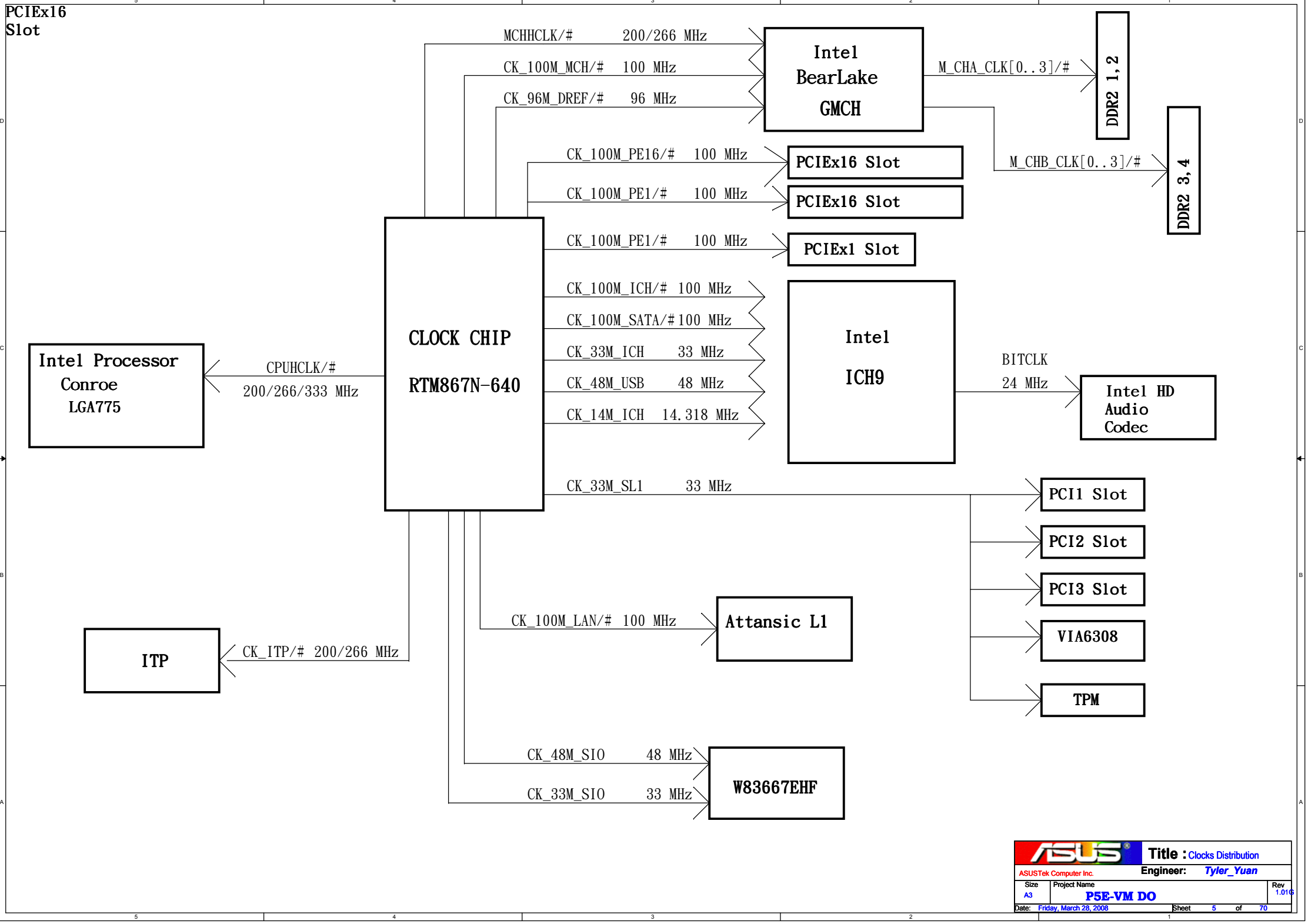
ASUSTek Computer Inc.

Title : Power Distribution

Engineer: Tyler_Yuan

Size	Project Name	Rev
A3	P5E-VM DO	1.01G

Date: Friday, March 28, 2008 Sheet 4 of 70



ASUSTek Computer Inc.

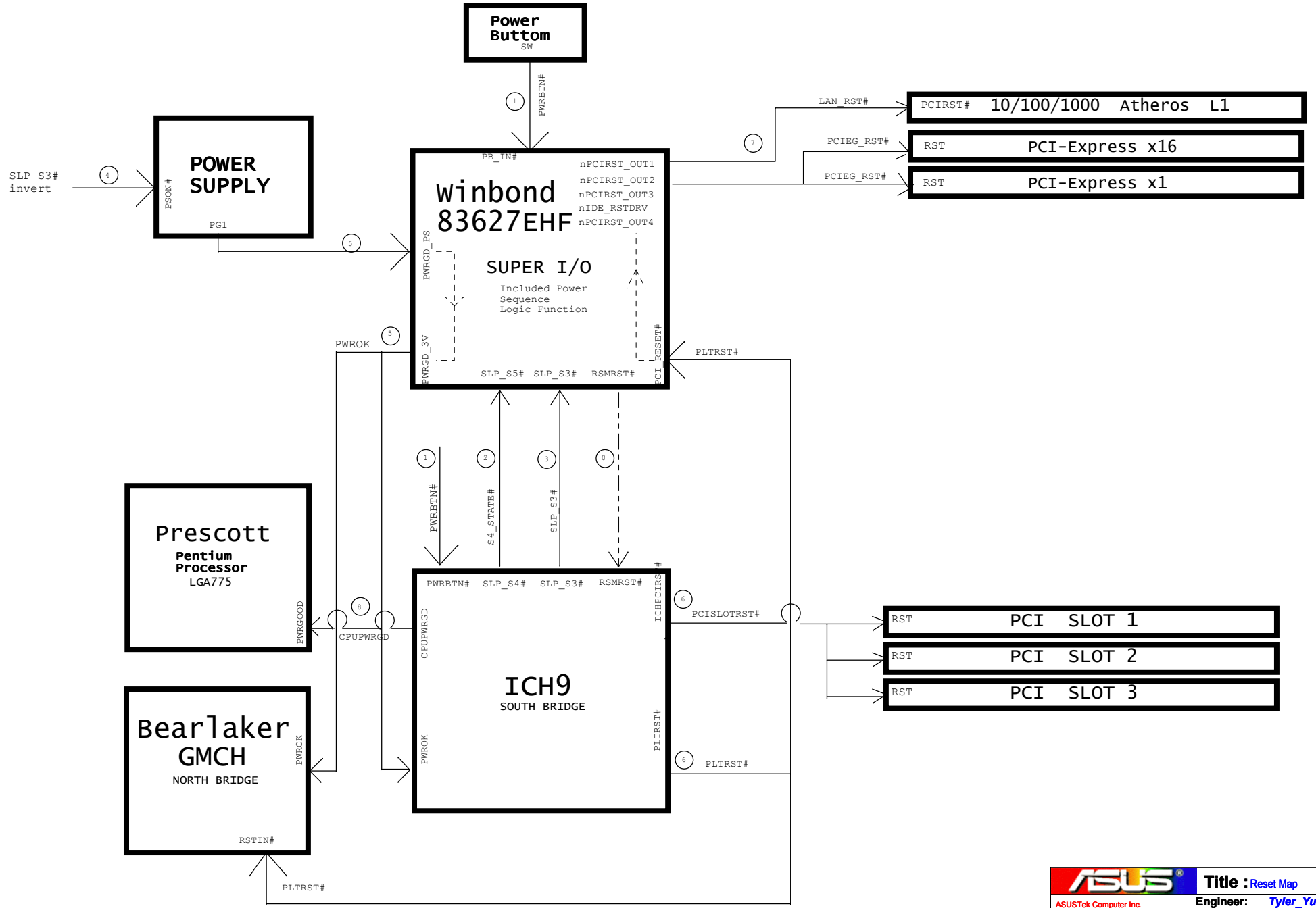
Title : Clocks Distribution

Engineer: Tyler_Yuan

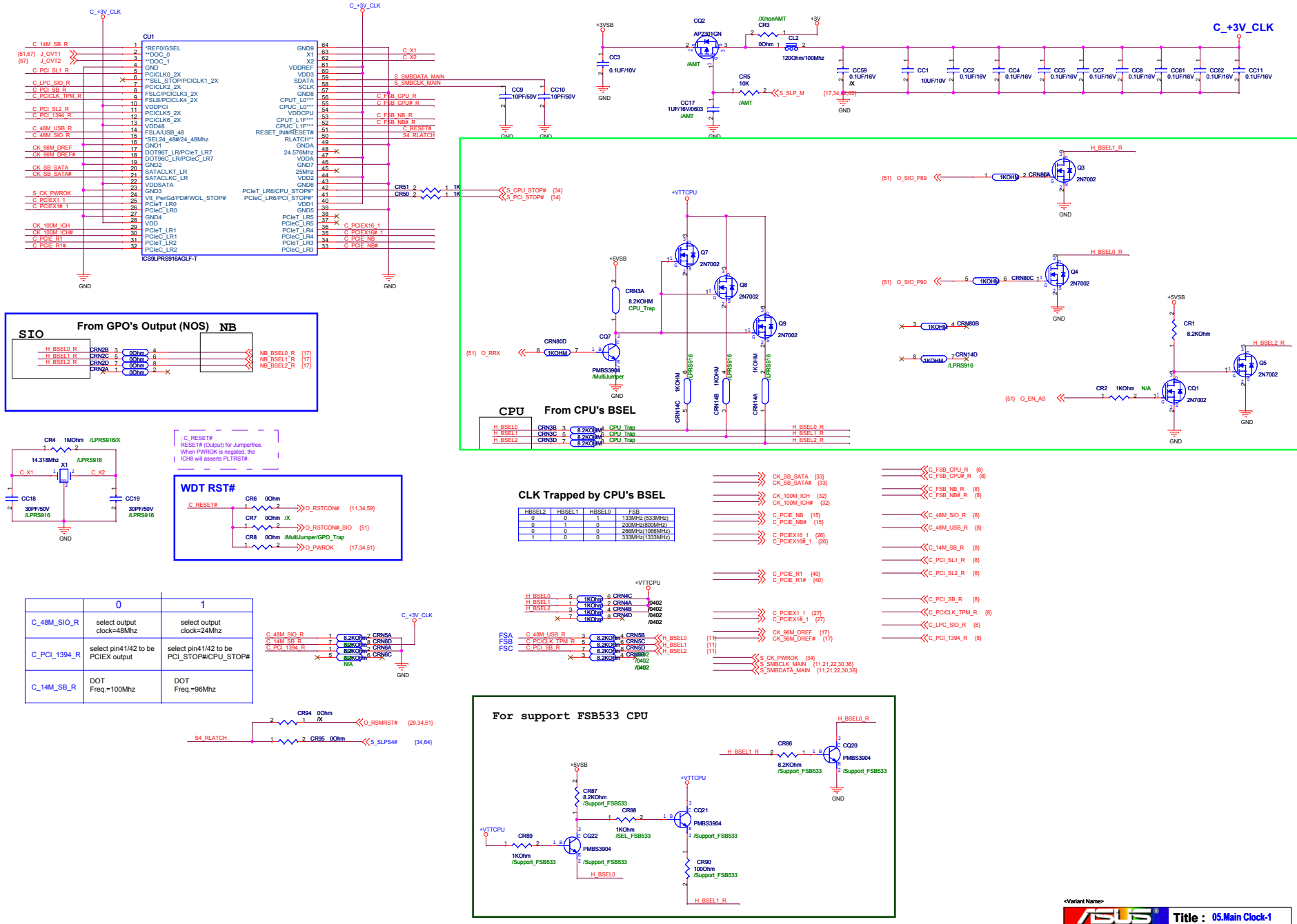
Size	Project Name	Rev
A3	P5E-VM DO	1.01G

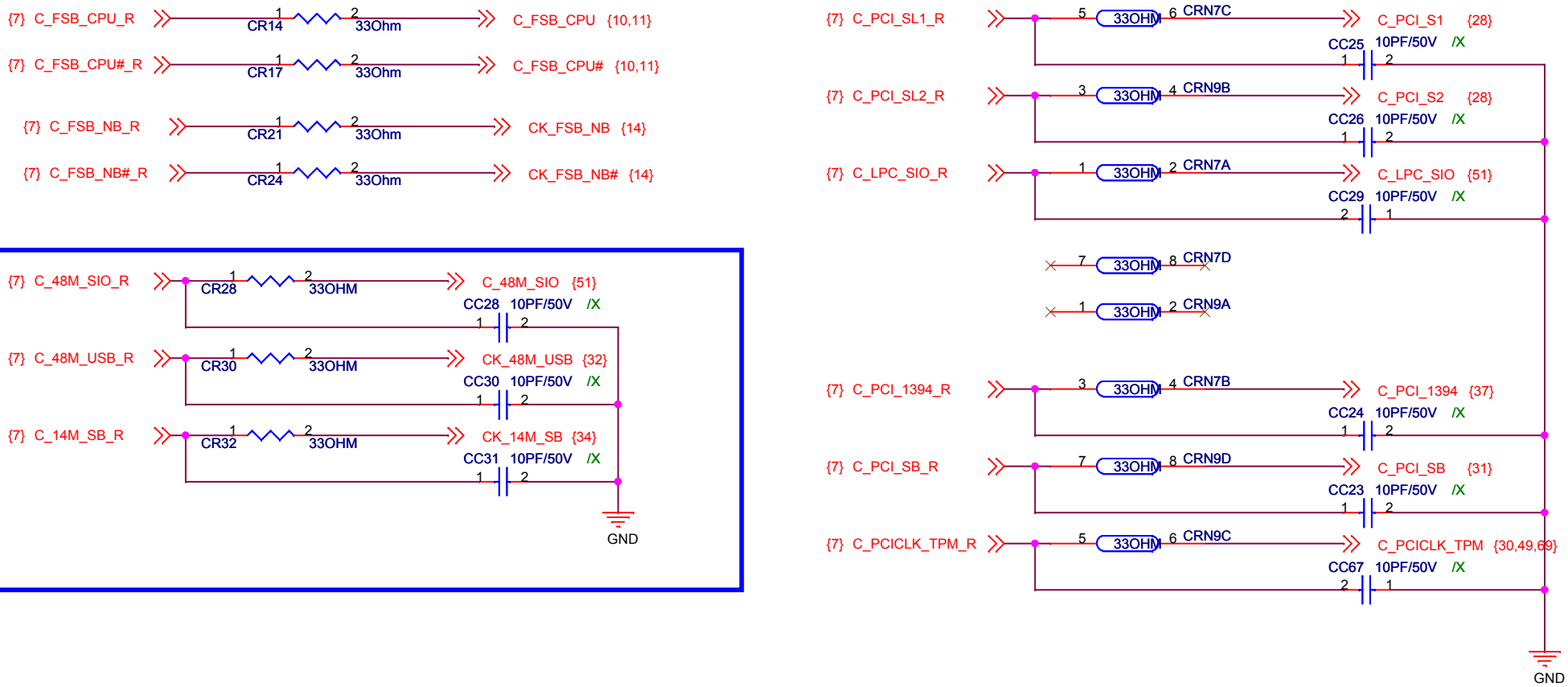
Date: Friday, March 28, 2008 Sheet 5 of 70

G0-to-G3 State Explain:
a. VCCSUS dirves high when PWR CONN plugd in.
b. RSMRST# drives high from SIO to ICH9.
c. SUSCLK sent out CLK from ICH9.



ASUSTek Computer Inc.	Title : Reset Map	
	Engineer: Tyler_Yuan	
Size: A3	Project Name: P5E-VM DO	Rev: 1.01G
Date: Friday, March 28, 2008	Sheet 6 of 70	


CU1
ICS9LPRS916AGLF-T
C_+3V_CLK
C_14M_SB_R
C_PCI_SL1_R
C_LPC_SIO_R
C_PCI_SB_R
C_PCICLK_TPM_R
C_PCI_SL2_R
C_PCI_1394_R
C_48M_USB_R
C_48M_SIO_R
CK_96M_DREF
CK_96M_DREF#
CK_SB_SATA
CK_SB_SATA#
S_CK_PWROK
C_PCIEX1_1
C_PCIEX1#_1
CK_100M_ICH
CK_100M_ICH#
C_PCIE_R1
C_PCIE_R1#
C_X1
C_X2
S_SMBDATA_MAIN
S_SMBCLK_MAIN
C_FSB_CPU_R
C_FSB_CPU#_R
C_FSB_NB_R
C_FSB_NB#_R
C_RESET#
S4_RLATCH
CR51
CR50
S_CPU_STOP#
S_PCI_STOP#
C_PCIEX16_1
C_PCIEX16#_1
C_PCIE_NB
C_PCIE_NB#
CC9
CC10
10PF/50V
GND
+3VSB
CC3
0.1UF/16V
CQ2
AP2301GN
/AMT
/KhonAMT
CR3
0Ohm
+3V
CL2
120Ohm/100Mhz
CR5
10K
S_SLP_M
{17,34,42,65}
CC17
1UF/16V/0603
CC59
/X
CC1
10UF/10V
CC2
CC4
CC5
CC7
CC8
CC81
CC82
CC11
0.1UF/16V
C_+3V_CLK
SIO
From GPO's Output (NOS)
NB
H_BSEL0_R
H_BSEL1_R
H_BSEL2_R
CRN2B
CRN2C
CRN2D
CRN2A
NB_BSEL0_R {17}
NB_BSEL1_R {17}
NB_BSEL2_R {17}
+VTTCPU
+5VSB
Q7
Q8
Q9
2N7002
CRN3A
8.2KOHM
CPU_Trap
CRN80D
1KOHM
CQ7
PMBS3904
/MultiJumper
{51} O_RRX
CPU
From CPU's BSEL
CRN3B
CRN3C
CRN3D
CRN14C
CRN14B
CRN14A
/LPRS916
H_BSEL1_R
Q3
{51} O_SIO_P89
CRN80A
H_BSEL0_R
Q4
{51} O_SIO_P90
CRN80C
CRN80B
CRN14D
CR1
8.2KOhm
Q5
CQ1
CR2
1KOhm
N/A
{51} O_EN_AS
H_BSEL2_R
CR4
1MOhm
/LPRS916/X
14.318Mhz
X1
CC18
CC19
30PF/50V
/LPRS916
; C_RESET#
RESET# (Output) for Jumperfree.
When PWROK is negated, the
ICH6 will asserts PLTRST#.
WDT RST#
CR6
CR7
CR8
/MultiJumper/GPO_Trap
O_RSTCON# {11,34,59}
O_RSTCON#_SIO {51}
O_PWROK {17,34,51}
CLK Trapped by CPU's BSEL
HBSEL2
HBSEL1
HBSEL0
FSB
133MHz (533MHz)
200MH2(800MHz)
266MH2(1066MHz)
333MH2(1333MHz)
CK_SB_SATA {33}
CK_SB_SATA# {33}
CK_100M_ICH {32}
CK_100M_ICH# {32}
C_PCIE_NB {15}
C_PCIE_NB# {15}
C_PCIEX16_1 {26}
C_PCIEX16#_1 {26}
C_PCIE_R1 {40}
C_PCIE_R1# {40}
C_PCIEX1_1 {27}
C_PCIEX1#_1 {27}
CK_96M_DREF {17}
CK_96M_DREF# {17}
S_CK_PWROK {34}
S_SMBCLK_MAIN {11,21,22,30,36}
S_SMBDATA_MAIN {11,21,22,30,36}
C_FSB_CPU_R {8}
C_FSB_CPU#_R {8}
C_FSB_NB_R {8}
C_FSB_NB#_R {8}
C_48M_SIO_R {8}
C_48M_USB_R {8}
C_14M_SB_R {8}
C_PCI_SL1_R {8}
C_PCI_SL2_R {8}
C_PCI_SB_R {8}
C_PCICLK_TPM_R {8}
C_LPC_SIO_R {8}
C_PCI_1394_R {8}
CRN4C
CRN4A
CRN4B
CRN4D
CRN5B
CRN5C
CRN5D
CRN5A
CRN6D
CRN6A
CRN6C
/0402
FSA
FSB
FSC
H_BSEL0 {11}
H_BSEL1 {11}
H_BSEL2 {11}
0 | 1
C_48M_SIO_R | select output clock=48Mhz | select output clock=24Mhz
C_PCI_1394_R | select pin41/42 to be PCIEX output | select pin41/42 to be PCI_STOP#/CPU_STOP#
C_14M_SB_R | DOT Freq.=100Mhz | DOT Freq.=96Mhz
CR94
CR95
O_RSMRST# {29,34,51}
S_SLPS4# {34,64}
For support FSB533 CPU
CR86
CQ20
CR87
CR88
CR89
CR90
CQ21
CQ22
/Support_FSB533
/SEL_FSB533
Title : 05.Main Clock-1
Engineer: Sdany_Shao
ASUSTek Computer Inc.
Size A2
Project Name P5E-VM DO
Rev 1.00
Date: Friday, March 28, 2008
Sheet 7 of 70



<Variant Name>

ASUSTek Computer Inc.	Title : 06.Main Clock-2	
	Engineer: Albert Chang	
Size: A4	Project Name: P5E-VM DO	Rev: 1.00
Date: Friday, March 28, 2008	Sheet 8 of 70	

0.2A Beta

```
CPU_GTLREF0/1/2/3 Voltage Divider for NVidia

 * CPU_GTLREF = 0.612 * VTT = 0.73V

 HR3 HR4 HR5 HR6 改爲 63.4
 HR7 HR8 HR9 HR10 改爲 100  10V213100110
CPU_GTLREF0/1/2/3 Voltage Divider for  intel 915~ 965,975

 * CPU_GTLREF = 0.63 * VTT = 0.75V
 HR3 HR4 HR5 HR6 改爲 124 10V213124110
 HR7 HR8 HR9 HR10 改爲 210 10V213210110

CPU_GTLREF0/1/2/3 Voltage Divider for X38 G35 945(for presler)

 * CPU_GTLREF = 0.67 * VTT = 0.8V

 HR3 HR4 HR5 HR6 改爲 100 10V213100110
 HR7 HR8 HR9 HR10 改爲 200 10V213210110
CPU_GTLREF0/1/2/3 Voltage Divider for Q35, Q33, G33,
P35, G31

 * CPU_GTLREF = 0.635 * VTT = 0.76V
HR3HR5 HR6 改爲 115 10G213115013010
 HR4  改爲57.6

HR7 HR9 HR10 改爲 200 10V213210110
HR8 改爲 100
```

LGA775A

8G support

Output, Not Stuff Close to CPU Len = 0~1.5".

Test Pin can remove for layout space

F2 is GTLREF3

Close to CPU

LGA775B

SOCKET775

<Variant Name>

Title :	LGA775-1 (Host Bus)
ASUS TeK Computer INC	Engineer: Makishin Huang
Size: A3	Project Name: P5E-VM DO
Rev: 0.2A	
Date: Friday, March 28, 2008	Sheet 9 of 70

0.2A Beta

LGA775C

+H_VTT_OUT_R

CPU VID Termination (CPU Side)

HRN8D HRN8C HRN8B HRN8A HRN9D HRN9C HRN9B HRN9A mb_4r8p0402 — 1KOhm

HR17 1KOhm 1% mb_r0402

{13,60} H_VID_SELECT
{51,60} H_VID0
{51,60} H_VID1
{51,60} H_VID2
{51,60} H_VID3
{51,60} H_VID4
{51,60} H_VID5
{51,60} H_VID6
{51,60} H_VID7

HRN2A HRN2B HRN2C HRN2D HRN1A HRN1B HRN1C HRN1D — 8.2KOhm — mb_4r8p0402

By SIO :8718 以 H_VID6_TBD,H_VID7_TBD 為 H_VIDI6,H_VIDI7. For winbond and other ITE SIO,以H_VID6,H_VID7

CPU Thermal Diode CAP
THERMDA : Ced. M. / Presler
PECI : Conroe

PECI Conreo / Allendale CPU Support

H_THERMTRIP# is O/D and need pull-high at SB side

If power didn't use,can be removed

INTEL SB and other : H_FERR# need pull-high at SB side

NVC55C19..H_FERR# 62ohm and H_NMI, H_INTR 150ohm need pull-high at SB side

{33} H_SMI#
{33} H_A20M#
{33} H_FERR#
{33} H_INTR
{33} H_NMI
{33} H_IGNNE#
{33} H_STPCLK#

P2 SMI#
K3 A20M#
R3 FERR#/PBE#
K1 LINT0/INTR
L1 LINT1/NMI
N2 IGNNE#
M3 STPCLK#

H_VID_SELECT — AN7 VID_SECECT
H_VID0_R — AM2 VID0
H_VID1_R — AL5 VID1
H_VID2_R — AM3 VID2
H_VID3_R — AL6 VID3
H_VID4_R — AK4 VID4
H_VID5_R — AL4 VID5
H_VID6_R — AM5 VID6
H_VID7_R — AM7 VID7

{8,11} C_FSB_CPU — F28 BCLK0
{8,11} C_FSB_CPU# — G28 BCLK1

{34} H_SKTOCC# — AE8 SKTOCC#

{51,55} H_THERM_CPU+ — AL1 THERMDA

HC11 100PF/50V NPO

{51,55} H_THERM_CPU- — HR62 0Ohm — H_THERM_CPU- R — AK1 THERMDC

HR63 0Ohm /X/775

GND {33} H_PECI — G5 PECI
{33} H_THERMTRIP# — M2 THERMTRIP#

AN3 VCC_SENSE
AN4 VSS_SENSE
AN5 VCC_MB_REGULATION
AN6 VSS_MB_REGULATION

+VCORE — AL8 VCC_D_SENSE
GND — AL7 VSS_D_SENSE

+VTTCPU

HL1 IND 0805 10UH 125mA 20% 10UH /X/775 — +H_VCCA — A23 VCCA
HL2 IND 0805 10UH 125mA 20% 10UH

HC12 10UF/10V

PLACE COMPONENTS AS CLOSE AS POSSIBLE TO CPU SOCKET. THE TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12 MIL.

HJP1 SHORTPIN /X/775

H_VSSA — B23 VSSA

HC13 10UF/10V

+VTTCPU
HL3 IND 0805 10UH 125mA 20% 10UH — +H_VCCIOPLL — C23 VCCIOPLL

H_VCCPLL

HL4 (CPU_FSB_PLLs_Power) 70Ohm/100Mhz mb_l0805 — H_VCC_PLL — D23 VCC_PLL

H_VCC_PLL from SB or other +1.5V in power page and need to care about the sequency.

H_VCC_PLL
New Feature for Conroe

HC15 10UF/10V /X/775
HC16 0.1UF/25V

C.D.:HC12/H13/H14/H15 change from 10uF/10V 1206 X7R to 10uF/10V 0805 Y5V by rule.

GND

+H_VTT_OUT_R

HR20-HR23 BOM should be by CPU support. Don't support old CPU,then BOM should change /X

+H_VTT_OUT_L

HR20 HR21 HR22 HR23 HR24 HR25 HR26 HR27 HR28 — 49.9Ohm — 24.9Ohm

H_COMP6 — Y3 COMP6
H_COMP7 — AE3 COMP7
H_COMP4 — J2 COMP4
H_COMP5 — T2 COMP5
H_COMP0 — A13 COMP0
H_COMP1 — T1 COMP1
H_COMP2 — G2 COMP2
H_COMP3 — R1 COMP3
H_COMP8 — B13 COMP8

H_COMP8 : 24.9ohm for PCB 50ohm
30.1ohm for PCB 60ohm

HC23 0.1UF/25V /X/775
HC17 0.1UF/25V /X/775

AJ7 RSVD7
AH7 RSVD8

SOCKET775

GND GND GND

TESTHI_2 F25 — H_TESTHI_2
TESTHI_3 G25 — H_TESTHI_3
TESTHI_4 G27 — H_TESTHI_4
TESTHI_5 G26 — H_TESTHI_5
TESTHI_6 G24 — H_TESTHI_6
TESTHI_7 F24 — H_TESTHI_7
TESTHI_0 F26 — H_TESTHI_0

HRN3A HR29 51Ohm mb_r0402 — +VTTCPU

+H_VTT_OUT_L

1.Close to CPU Len = 0 ~ 3 in.
2. VC is 62 Ohm

HRN3D HRN3C HRN3B — 51Ohm

TESTHI08 G3 — H_TESTHI_8 {11}
TESTHI09 G4 — H_TESTHI_9 {11}
TESTHI10 H5 — H_TESTHI_10

+H_VTT_OUT_L

TESTHI_1 W3 — H_TESTHI_1
TESTHI_11 P1 — H_TESTHI_11
TESTHI_12 W2 — H_TESTHI_12
TESTHI_13 L2 — H_TESTHI_13

HRN4B HRN4D HRN4A HRN4C — 51Ohm

RSVD34 U1 — H_TESTHI_12

Connected to Pin "TESTHI_12"

Depend on chipset support : Connected to SB CPUSLP# ICH8: can disconnect

+H_VTT_OUT_L

RSVD33 G1 — H_TP_CPU_G1 — HR30 51Ohm mb_r0402 — H_TP_CPU_G1 {11}
RSVD35 A24 — H_TP_DCKLPH_A24 — HR31 1KOhm /X/775
RSVD36 E29 — H_TP_SFRANAD2_E29 — HT41 /X/775 1% mb_r0402
RSVD12 AH2 — H_TP_CPU_AH2 — HT18 /X/775
BOOTSELECT Y1 — H_CPUBOOT — HR64 51Ohm /X/775 mb_r0402 — H_CPUBOOT {13}
RSVD9 F29 — H_TP_RSD_E29 — HT29 /X/775
RSVD21 G6 — H_TP_SLEWCTRL_G6 — HT17 /X/775
LL_ID0 V2 — H_TP_LL_ID0_V2 — HT26 /X/775
LL_ID1 AA2 — H_TP_LL_ID1_AA2 — HT30 /X/775
NC AL3 — H_TP_VRDSEL — HT42 /X/775

GND

BL_support
BOOTSELECT Y1: Weak
Internal PU

	2005P	2005V	06(65W)
MSID1	GND	GND	GND
MSID0	GND	NC	NC

+H_VTT_OUT_R

RESET# G23 — H_CPURST# — HR32 62Ohm mb_r0402 — H_CPURST# {11,14}

HR32 : Close to CPU Len = 0 ~ 3 in.

+H_VTT_OUT_L

PWRGOOD N1 — H_CPUPWRGD — HR33 100Ohm /X/775 — H_CPUPWRGD {11,34}

HR33 : Intel CRB Remove it

+H_VTT_OUT_R

PROCHOT# AL2 — H_PROCHOT# — HR34 120Ohm 1% — H_PROCHOT# {60,67}

H_PROCHOT#:If use the input and output function,need to PU

+H_VTT_OUT_R

FORCEPR# AK6 — H_FORCEPR# — HR35 120Ohm 1% — H_FORCEPR# {60,67}

H_FORCEPR#,H_PROCHOT# : Use for Dual-Core CPU VR Thermal Control Circuit(TCC)

IMPSEL F6 — H_IMPSEL — HR36 51Ohm mb_r0402

HR36: 51ohm for 1080, NC for 2116

MSID1 V1 — H_MSID1
MSID0 W1 — H_MSID0 — H_MSID0 {13}

HR37 51Ohm mb_r0402
HR38 51Ohm mb_r0402

HR37 HR38 bom by design. Default 05P

GND GND

<Variant Name>

ASUS

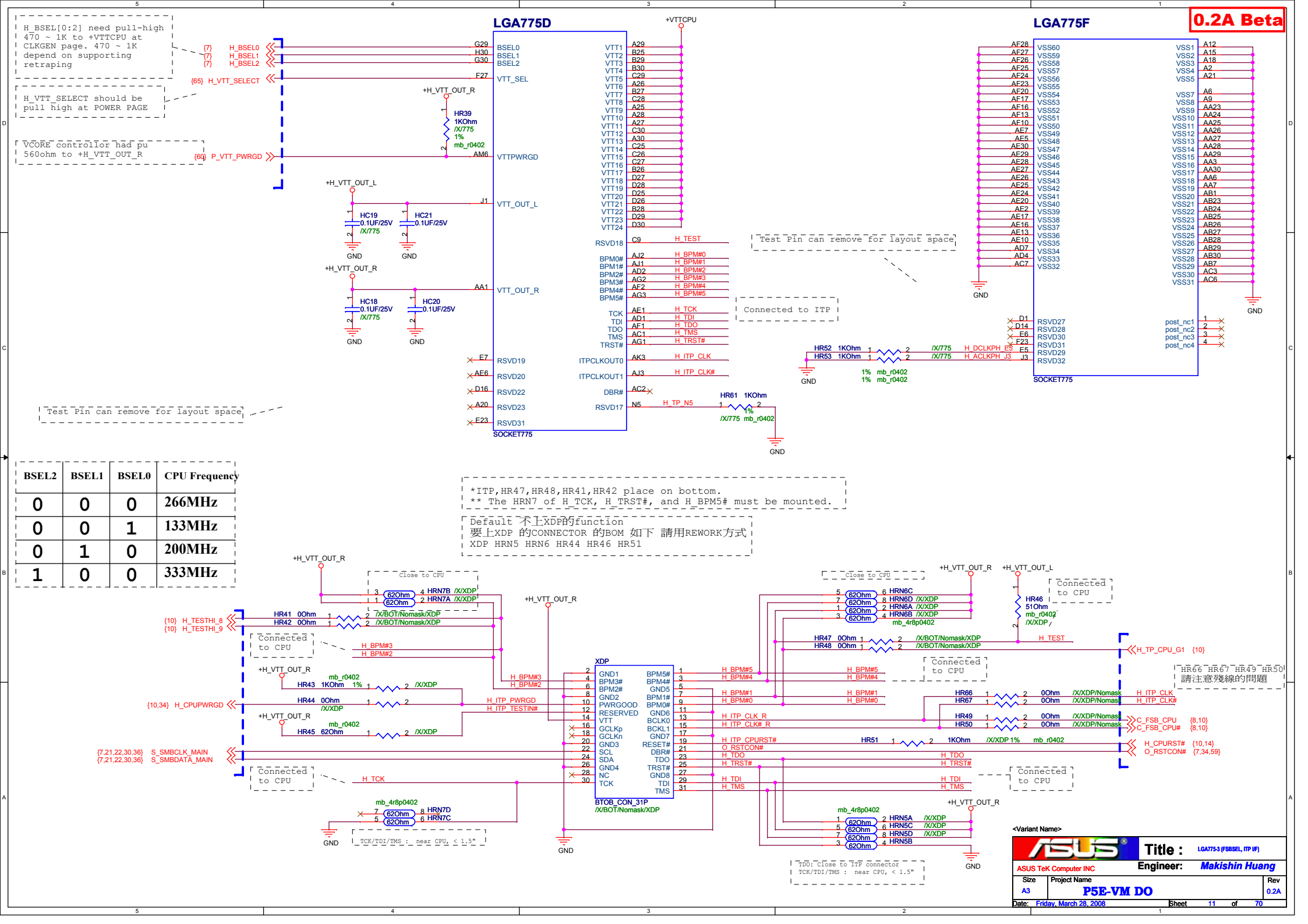
Title : LGA775-2 (CPU, VID, Misc.)

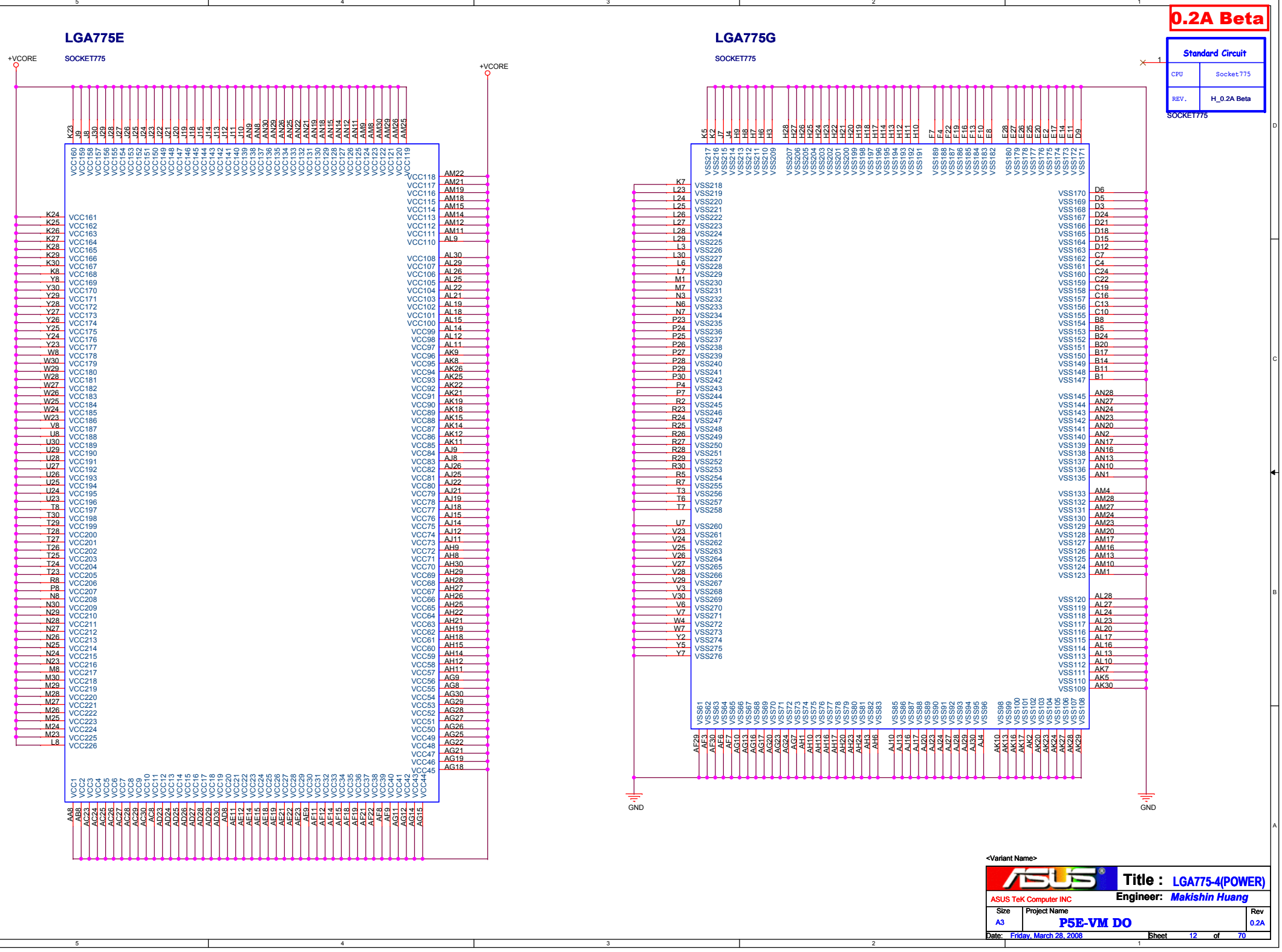
ASUS TeK Computer INC

Engineer: Makishin Huang

Size	Project Name	Rev
A3	P5E-VM DO	0.2A

Date: Friday, March 28, 2008 Sheet 10 of 70


0.2A Beta
LGA775D
LGA775F
H_BSEL[0:2] need pull-high 470 ~ 1K to +VTTCPU at CLKGEN page. 470 ~ 1K depend on supporting retraping
H_VTT_SELECT should be pull high at POWER PAGE
VCORE controllor had pu 560ohm to +H_VTT_OUT_R
Test Pin can remove for layout space
Connected to ITP
SOCKET775
BSEL2 BSEL1 BSEL0 CPU Frequency
0 0 0 266MHz
0 0 1 133MHz
0 1 0 200MHz
1 0 0 333MHz
*ITP,HR47,HR48,HR41,HR42 place on bottom.
** The HRN7 of H_TCK, H_TRST#, and H_BPM5# must be mounted.
Default 不上XDP的function
要上XDP 的CONNECTOR 的BOM 如下 請用REWORK方式
XDP HRN5 HRN6 HR44 HR46 HR51
Close to CPU
Connected to CPU
BTOB_CON_31P
/X/BOT/Nomask/XDP
TCK/TDI/TMS : near CPU, < 1.5"
TDO: Close to ITP connector
TCK/TDI/TMS : near CPU, < 1.5"
HR66 HR67 HR49 HR50
請注意殘線的問題
<Variant Name>
ASUS TeK Computer INC
Title : LGA775-3 (FSBSEL, ITP I/F)
Engineer: Makishin Huang
Size A3
Project Name P5E-VM DO
Rev 0.2A
Date: Friday, March 28, 2008
Sheet 11 of 70


0.2A Beta
Standard Circuit
CPU
Socket775
REV.
H_0.2A Beta
LGA775E
SOCKET775
+VCORE
LGA775G
SOCKET775
GND
<Variant Name>
Title : LGA775-4(POWER)
ASUS TeK Computer INC
Engineer: Makishin Huang
Size
A3
Project Name
P5E-VM DO
Rev
0.2A
Date: Friday, March 28, 2008
Sheet 12 of 70

0.2A Beta

NEW CPU SWITCH (Conroe ,Wolfdale)

	VRD10.1	VRD11
H_VID_SELECT	GND	HIGH
H_CPUBOOT	FLOATING	GND
H_MSID0	GND	FLOATING

GTLREF over Voltage circuit (Yorkfield,Wolfdale)

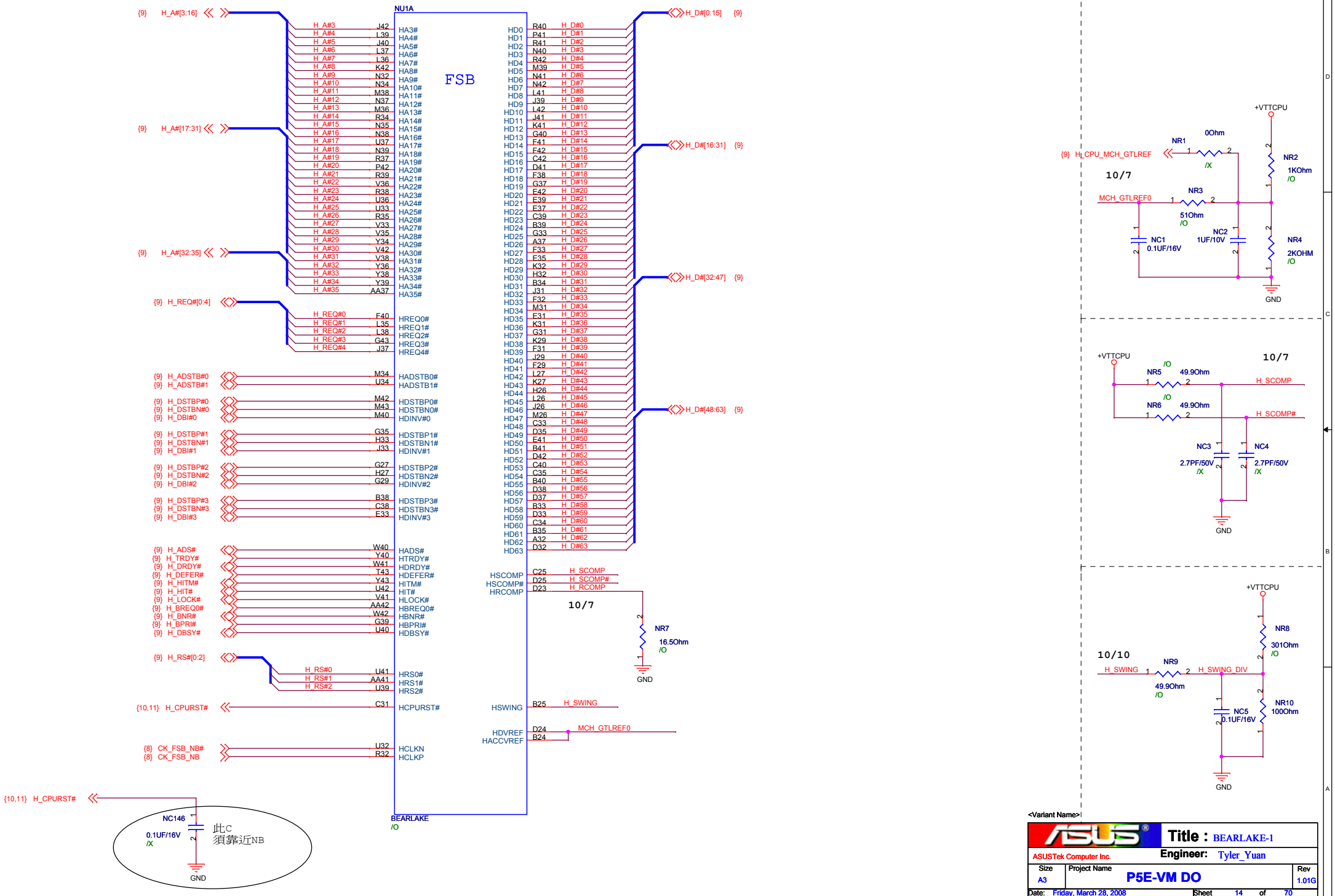
GPIO-I.Default Input PIN with standby power
2.Default output high PIN with standby power

This table only for Q35, Q33, G33, P35, G31
Other is TBD

OV3	OV2	OV1	Ratio Set
1	1	1	0.635
	1	0	0.618
	0	1	0.597
	0	0	0.581
0	1	1	0.576
	1	0	0.561
	0	1	0.545
	0	0	0.531

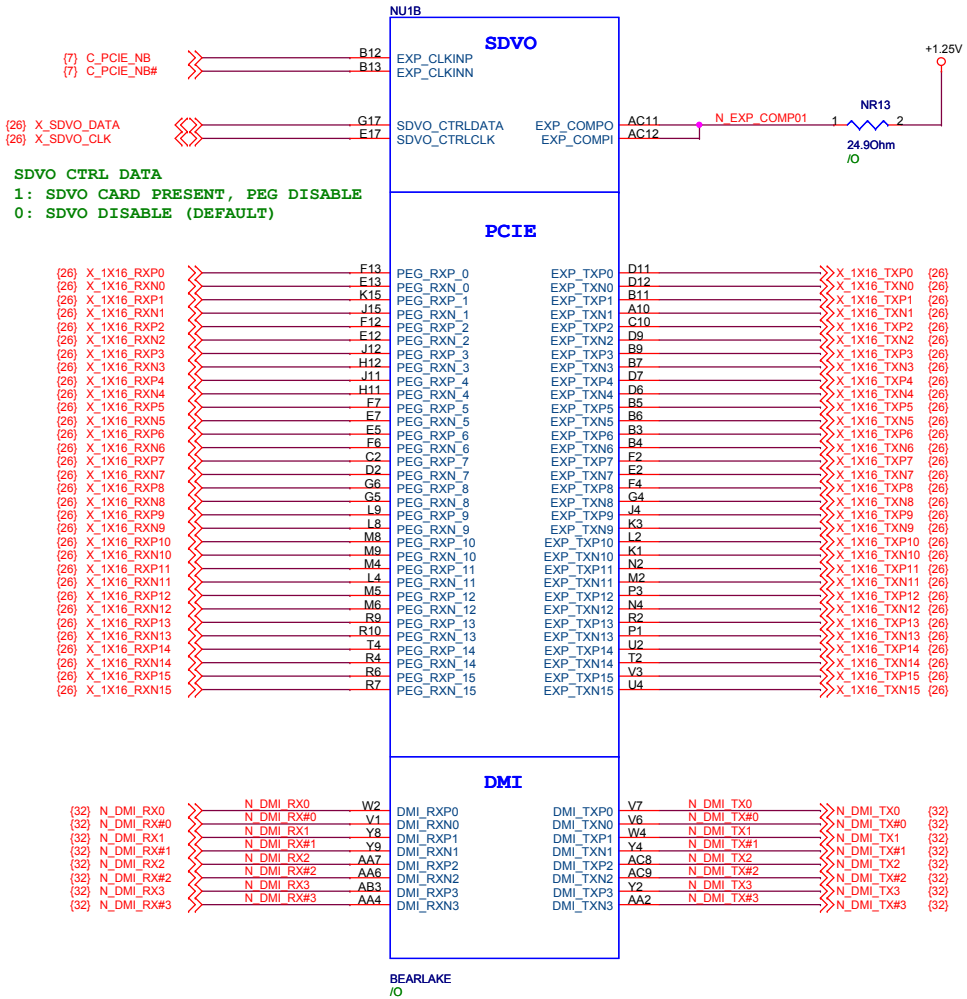
<Variant Name>

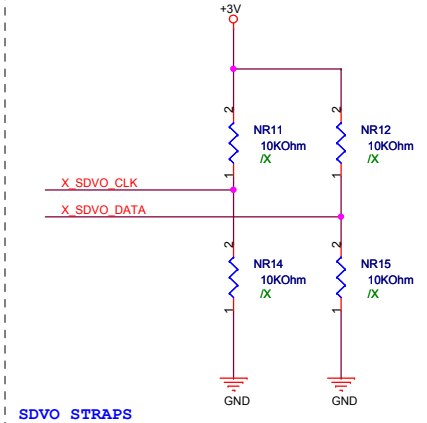
Title : LGA775-5(SWITCH)
ASUS TeK Computer INC
Engineer: Makishin Huang
Size: A3 | Project Name: P5E-VM DO | Rev: 0.2A
Date: Friday, March 28, 2008 | Sheet 13 of 70



<Variant Name>

ASUSTek Computer Inc.	Title : BEARLAKE-1	
	Engineer: Tyler_Yuan	
Size: A3	Project Name: P5E-VM DO	Rev: 1.01G
Date: Friday, March 28, 2008	Sheet 14 of 70	

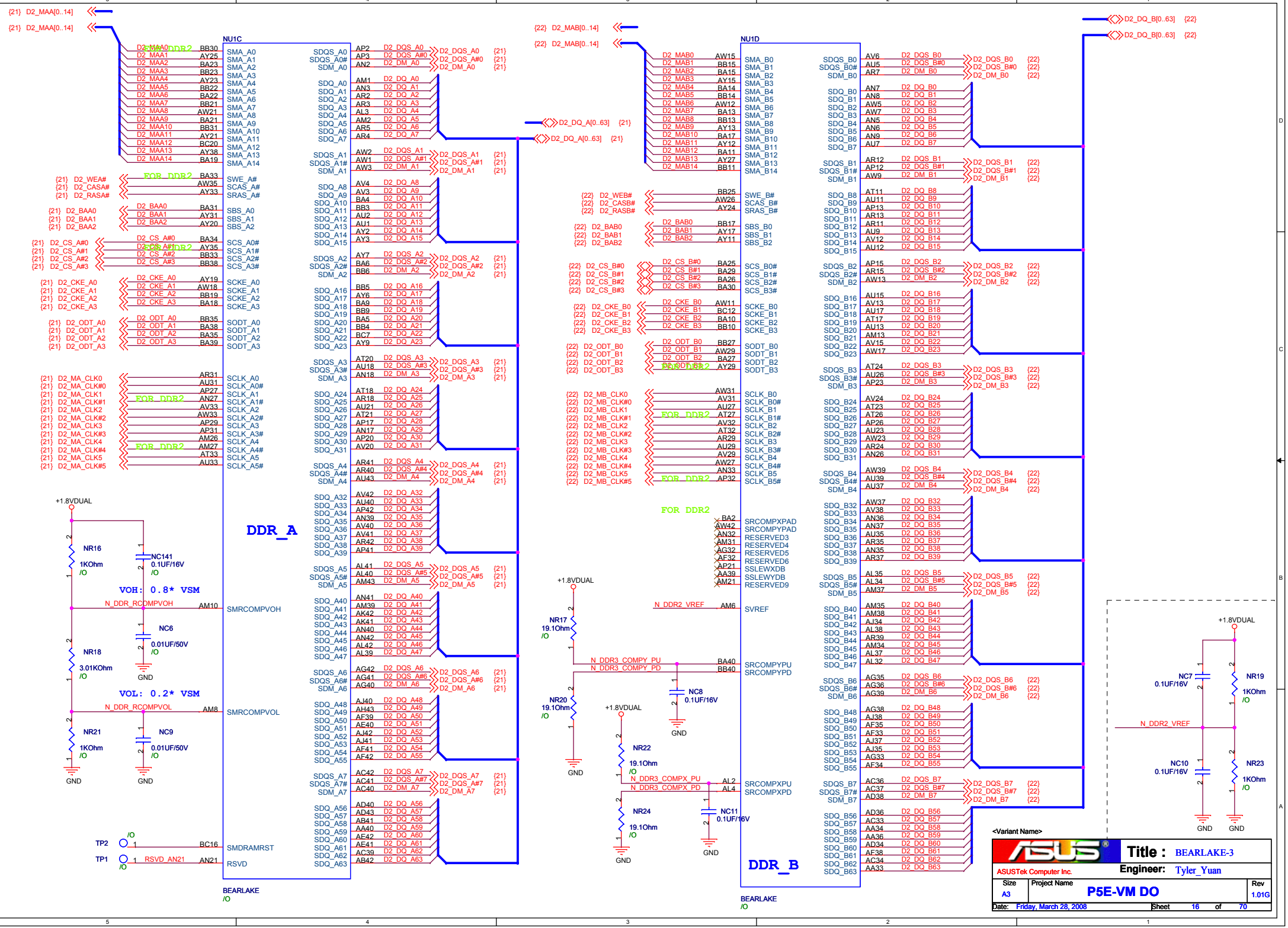




SDVO CTRL DATA
1: SDVO CARD PRESENT, PEG DISABLE
0: SDVO DISABLE (DEFAULT)

<Variant Name>

ASUSTek Computer Inc.	Title : BEARLAKE-2	
	Engineer: Tyler_Yuan	
Size: A3	Project Name: P5E-VM DO	Rev: 1.01G
Date: Friday, March 28, 2008	Sheet 15 of 70	


NU1C
DDR_A
BEARLAKE
/O
NU1D
DDR_B
BEARLAKE
/O
FOR DDR2
SMA_A0
SMA_A1
SMA_A2
SMA_A3
SMA_A4
SMA_A5
SMA_A6
SMA_A7
SMA_A8
SMA_A9
SMA_A10
SMA_A11
SMA_A12
SMA_A13
SMA_A14
SWE_A#
SCAS_A#
SRAS_A#
SBS_A0
SBS_A1
SBS_A2
SCS_A0#
SCS_A1#
SCS_A2#
SCS_A3#
SCKE_A0
SCKE_A1
SCKE_A2
SCKE_A3
SODT_A0
SODT_A1
SODT_A2
SODT_A3
SCLK_A0
SCLK_A0#
SCLK_A1
SCLK_A1#
SCLK_A2
SCLK_A2#
SCLK_A3
SCLK_A3#
SCLK_A4
SCLK_A4#
SCLK_A5
SCLK_A5#
SMRCOMPVOH
SMRCOMPVOL
SMDRAMRST
RSVD
SDQS_A0
SDQS_A0#
SDM_A0
SDQ_A0
SDQ_A1
SDQ_A2
SDQ_A3
SDQ_A4
SDQ_A5
SDQ_A6
SDQ_A7
SDQS_A1
SDQS_A1#
SDM_A1
SDQ_A8
SDQ_A9
SDQ_A10
SDQ_A11
SDQ_A12
SDQ_A13
SDQ_A14
SDQ_A15
SDQS_A2
SDQS_A2#
SDM_A2
SDQ_A16
SDQ_A17
SDQ_A18
SDQ_A19
SDQ_A20
SDQ_A21
SDQ_A22
SDQ_A23
SDQS_A3
SDQS_A3#
SDM_A3
SDQ_A24
SDQ_A25
SDQ_A26
SDQ_A27
SDQ_A28
SDQ_A29
SDQ_A30
SDQ_A31
SDQS_A4
SDQS_A4#
SDM_A4
SDQ_A32
SDQ_A33
SDQ_A34
SDQ_A35
SDQ_A36
SDQ_A37
SDQ_A38
SDQ_A39
SDQS_A5
SDQS_A5#
SDM_A5
SDQ_A40
SDQ_A41
SDQ_A42
SDQ_A43
SDQ_A44
SDQ_A45
SDQ_A46
SDQ_A47
SDQS_A6
SDQS_A6#
SDM_A6
SDQ_A48
SDQ_A49
SDQ_A50
SDQ_A51
SDQ_A52
SDQ_A53
SDQ_A54
SDQ_A55
SDQS_A7
SDQS_A7#
SDM_A7
SDQ_A56
SDQ_A57
SDQ_A58
SDQ_A59
SDQ_A60
SDQ_A61
SDQ_A62
SDQ_A63
D2_DQS_A0
D2_DQS_A#0
D2_DM_A0
D2_DQ_A0
D2_DQ_A1
D2_DQ_A2
D2_DQ_A3
D2_DQ_A4
D2_DQ_A5
D2_DQ_A6
D2_DQ_A7
D2_DQS_A1
D2_DQS_A#1
D2_DM_A1
D2_DQ_A8
D2_DQ_A9
D2_DQ_A10
D2_DQ_A11
D2_DQ_A12
D2_DQ_A13
D2_DQ_A14
D2_DQ_A15
D2_DQS_A2
D2_DQS_A#2
D2_DM_A2
D2_DQ_A16
D2_DQ_A17
D2_DQ_A18
D2_DQ_A19
D2_DQ_A20
D2_DQ_A21
D2_DQ_A22
D2_DQ_A23
D2_DQS_A3
D2_DQS_A#3
D2_DM_A3
D2_DQ_A24
D2_DQ_A25
D2_DQ_A26
D2_DQ_A27
D2_DQ_A28
D2_DQ_A29
D2_DQ_A30
D2_DQ_A31
D2_DQS_A4
D2_DQS_A#4
D2_DM_A4
D2_DQ_A32
D2_DQ_A33
D2_DQ_A34
D2_DQ_A35
D2_DQ_A36
D2_DQ_A37
D2_DQ_A38
D2_DQ_A39
D2_DQS_A5
D2_DQS_A#5
D2_DM_A5
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D2_DQ_A42
D2_DQ_A43
D2_DQ_A44
D2_DQ_A45
D2_DQ_A46
D2_DQ_A47
D2_DQS_A6
D2_DQS_A#6
D2_DM_A6
D2_DQ_A48
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D2_DQ_A53
D2_DQ_A54
D2_DQ_A55
D2_DQS_A7
D2_DQS_A#7
D2_DM_A7
D2_DQ_A56
D2_DQ_A57
D2_DQ_A58
D2_DQ_A59
D2_DQ_A60
D2_DQ_A61
D2_DQ_A62
D2_DQ_A63
D2_DQ_A[0..63]
D2_MAA[0..14]
D2_MAB[0..14]
D2_DQ_B[0..63]
SMA_B0
SMA_B1
SMA_B2
SMA_B3
SMA_B4
SMA_B5
SMA_B6
SMA_B7
SMA_B8
SMA_B9
SMA_B10
SMA_B11
SMA_B12
SMA_B13
SMA_B14
SWE_B#
SCAS_B#
SRAS_B#
SBS_B0
SBS_B1
SBS_B2
SCS_B0#
SCS_B1#
SCS_B2#
SCS_B3#
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SCKE_B1
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SCKE_B3
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SODT_B3
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SCLK_B0#
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SCLK_B2#
SCLK_B3
SCLK_B3#
SCLK_B4
SCLK_B4#
SCLK_B5
SCLK_B5#
SRCOMPXPAD
SRCOMPYPAD
RESERVED3
RESERVED4
RESERVED5
RESERVED6
SSLEWXDB
SSLEWYDB
RESERVED9
SVREF
SRCOMPYPU
SRCOMPYPD
SRCOMPXPU
SRCOMPXPD
SDQS_B0
SDQS_B0#
SDM_B0
SDQ_B0
SDQ_B1
SDQ_B2
SDQ_B3
SDQ_B4
SDQ_B5
SDQ_B6
SDQ_B7
SDQS_B1
SDQS_B1#
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SDQ_B15
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SDQS_B2#
SDM_B2
SDQ_B16
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SDQ_B18
SDQ_B19
SDQ_B20
SDQ_B21
SDQ_B22
SDQ_B23
SDQS_B3
SDQS_B3#
SDM_B3
SDQ_B24
SDQ_B25
SDQ_B26
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SDQ_B59
SDQ_B60
SDQ_B61
SDQ_B62
SDQ_B63
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D2_DQS_B#0
D2_DM_B0
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D2_DQ_B38
D2_DQ_B39
D2_DQS_B5
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D2_DQS_B6
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D2_DQ_B50
D2_DQ_B51
D2_DQ_B52
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D2_DQ_B54
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D2_DQS_B7
D2_DQS_B#7
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D2_DQ_B62
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D2_RASB#
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D2_BAB1
D2_BAB2
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D2_CS_B#1
D2_CS_B#2
D2_CS_B#3
D2_CKE_B0
D2_CKE_B1
D2_CKE_B2
D2_CKE_B3
D2_ODT_B0
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D2_ODT_B2
D2_ODT_B3
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D2_MB_CLK#0
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D2_MB_CLK#1
D2_MB_CLK2
D2_MB_CLK#2
D2_MB_CLK3
D2_MB_CLK#3
D2_MB_CLK4
D2_MB_CLK#4
D2_MB_CLK5
D2_MB_CLK#5
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N_DDR3_COMPX_PD
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D2_BAA1
D2_BAA2
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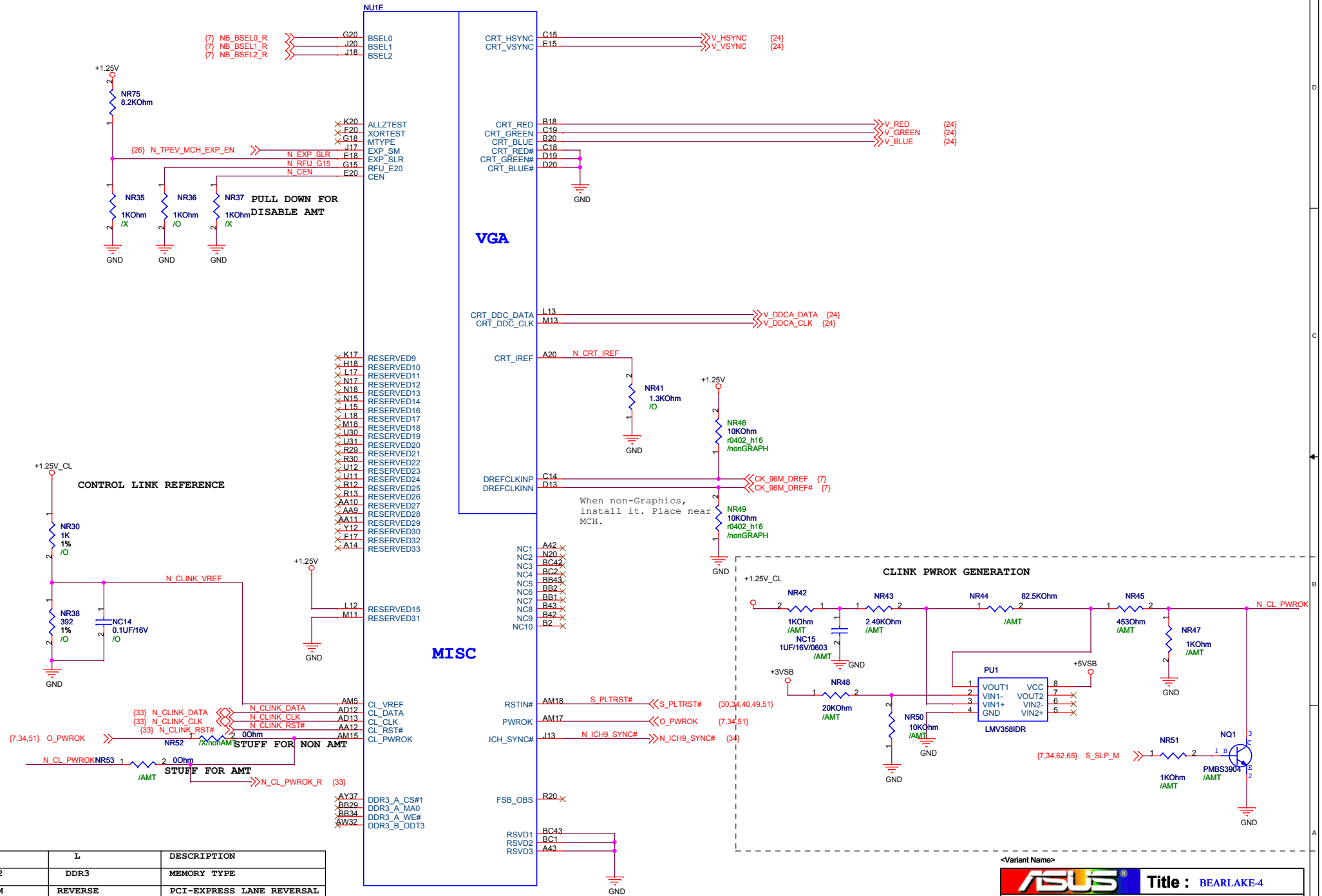
D2_CS_A#1
D2_CS_A#2
D2_CS_A#3
D2_CKE_A0
D2_CKE_A1
D2_CKE_A2
D2_CKE_A3
D2_ODT_A0
D2_ODT_A1
D2_ODT_A2
D2_ODT_A3
D2_MA_CLK0
D2_MA_CLK#0
D2_MA_CLK1
D2_MA_CLK#1
D2_MA_CLK2
D2_MA_CLK#2
D2_MA_CLK3
D2_MA_CLK#3
D2_MA_CLK4
D2_MA_CLK#4
D2_MA_CLK5
D2_MA_CLK#5
+1.8VDUAL
NR16
1KOhm
/O
NC141
0.1UF/16V
/O
VOH: 0.8* VSM
N_DDR_RCOMPVOH
NC6
0.01UF/50V
/O
NR18
3.01KOhm
/O
VOL: 0.2* VSM
N_DDR_RCOMPVOL
NR21
1KOhm
/O
NC9
0.01UF/50V
/O
GND
TP2
TP1
RSVD_AN21
NR17
19.1Ohm
/O
NC8
0.1UF/16V
NR20
19.1Ohm
/O
NR22
19.1Ohm
/O
NR24
19.1Ohm
/O
NC11
0.1UF/16V
NC7
0.1UF/16V
NR19
1KOhm
/O
NC10
0.1UF/16V
NR23
1KOhm
/O
<Variant Name>
Title : BEARLAKE-3
ASUSTek Computer Inc.
Engineer: Tyler_Yuan
Size
A3
Project Name
P5E-VM DO
Rev
1.01G
Date: Friday, March 28, 2008
Sheet 16 of 70



Pin	H	L	DESCRIPTION
MTYPE	DDR2	DDR3	MEMORY TYPE
EXP_SLR	NORM	REVERSE	PCI-EXPRESS LANE REVERSAL
EXP_EN	CONCURRENT	NON-CONCURRENT	PCI-E / SDVO CO-EXISTENCE
TCEN	ENABLE	DISABLE	TLS CONFIDENTIALITY

<Variant Name>

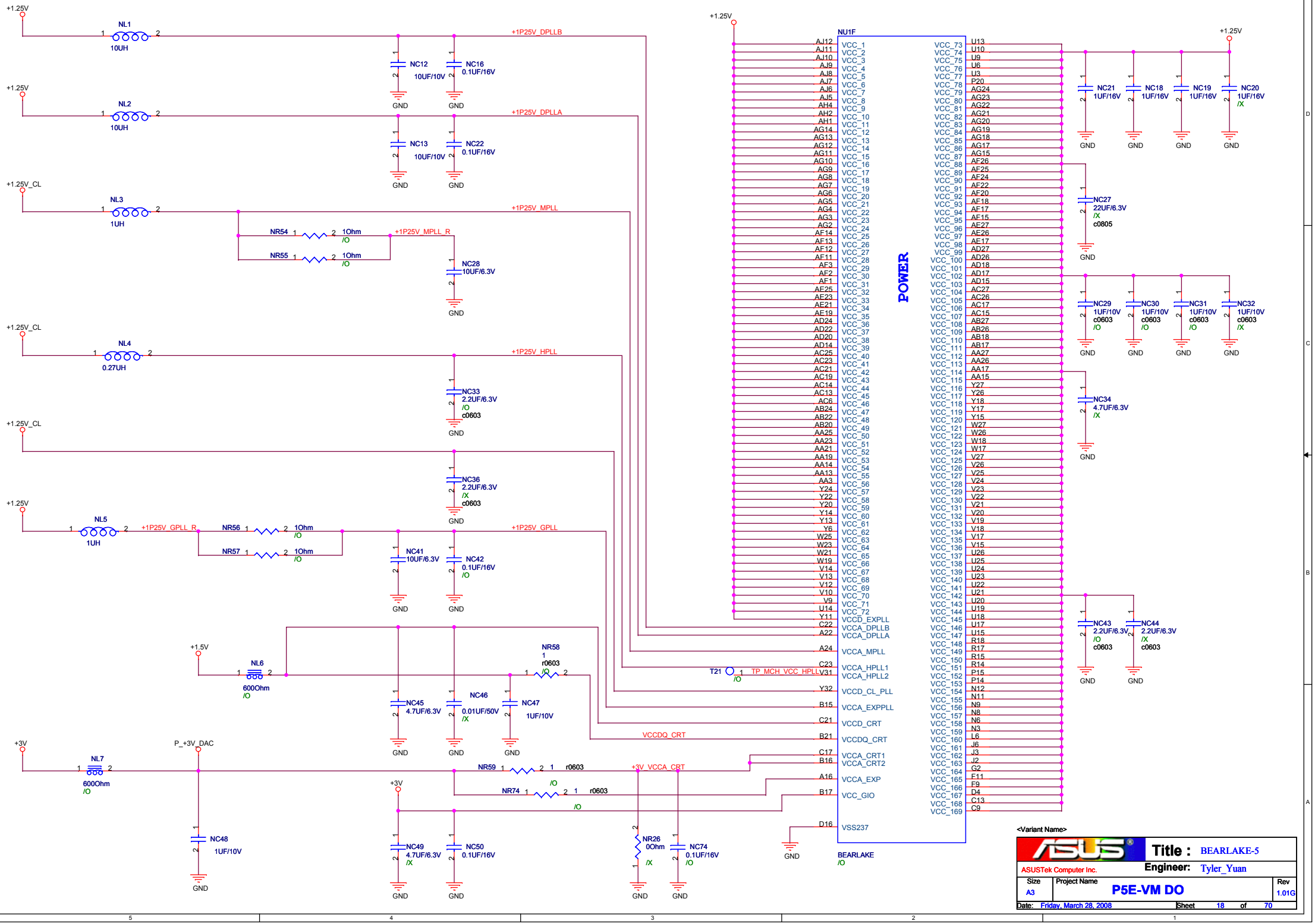
ASUSTek Computer Inc.

Title : BEARLAKE-4

Engineer: Tyler_Yuan

Size	Project Name	Rev
A3	P5E-VM DO	1.01G

Date: Friday, March 28, 2008 Sheet 17 of 70


+1.25V
NL1
10UH
NC12
10UF/10V
NC16
0.1UF/16V
GND
+1P25V_DPLLB
NL2
10UH
NC13
10UF/10V
NC22
0.1UF/16V
+1P25V_DPLLA
+1.25V_CL
NL3
1UH
NR54
NR55
1Ohm
/O
+1P25V_MPLL_R
+1P25V_MPLL
NC28
10UF/6.3V
NL4
0.27UH
NC33
2.2UF/6.3V
c0603
+1P25V_HPLL
NC36
2.2UF/6.3V
/X
NL5
1UH
+1P25V_GPLL_R
NR56
NR57
NC41
10UF/6.3V
NC42
0.1UF/16V
+1P25V_GPLL
+1.5V
NL6
600Ohm
NR58
r0603
NC45
4.7UF/6.3V
NC46
0.01UF/50V
NC47
1UF/10V
VCCDQ_CRT
+3V
NL7
600Ohm
P_+3V_DAC
NC48
1UF/10V
NR59
+3V_VCCA_CRT
NR74
NC49
4.7UF/6.3V
NC50
0.1UF/16V
NR26
0Ohm
NC74
0.1UF/16V
NU1F
POWER
VCC_1
VCC_2
VCC_3
VCC_4
VCC_5
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
VCC_14
VCC_15
VCC_16
VCC_17
VCC_18
VCC_19
VCC_20
VCC_21
VCC_22
VCC_23
VCC_24
VCC_25
VCC_26
VCC_27
VCC_28
VCC_29
VCC_30
VCC_31
VCC_32
VCC_33
VCC_34
VCC_35
VCC_36
VCC_37
VCC_38
VCC_39
VCC_40
VCC_41
VCC_42
VCC_43
VCC_44
VCC_45
VCC_46
VCC_47
VCC_48
VCC_49
VCC_50
VCC_51
VCC_52
VCC_53
VCC_54
VCC_55
VCC_56
VCC_57
VCC_58
VCC_59
VCC_60
VCC_61
VCC_62
VCC_63
VCC_64
VCC_65
VCC_66
VCC_67
VCC_68
VCC_69
VCC_70
VCC_71
VCC_72
VCCD_EXPLL
VCCA_DPLLB
VCCA_DPLLA
VCCA_MPLL
VCCA_HPLL1
VCCA_HPLL2
VCCD_CL_PLL
VCCA_EXPPLL
VCCD_CRT
VCCDQ_CRT
VCCA_CRT1
VCCA_CRT2
VCCA_EXP
VCC_GIO
VSS237
BEARLAKE
/O
T21
TP_MCH_VCC_HPLL
VCC_73
VCC_74
VCC_75
VCC_76
VCC_77
VCC_78
VCC_79
VCC_80
VCC_81
VCC_82
VCC_83
VCC_84
VCC_85
VCC_86
VCC_87
VCC_88
VCC_89
VCC_90
VCC_91
VCC_92
VCC_93
VCC_94
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VCC_112
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VCC_115
VCC_116
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VCC_135
VCC_136
VCC_137
VCC_138
VCC_139
VCC_140
VCC_141
VCC_142
VCC_143
VCC_144
VCC_145
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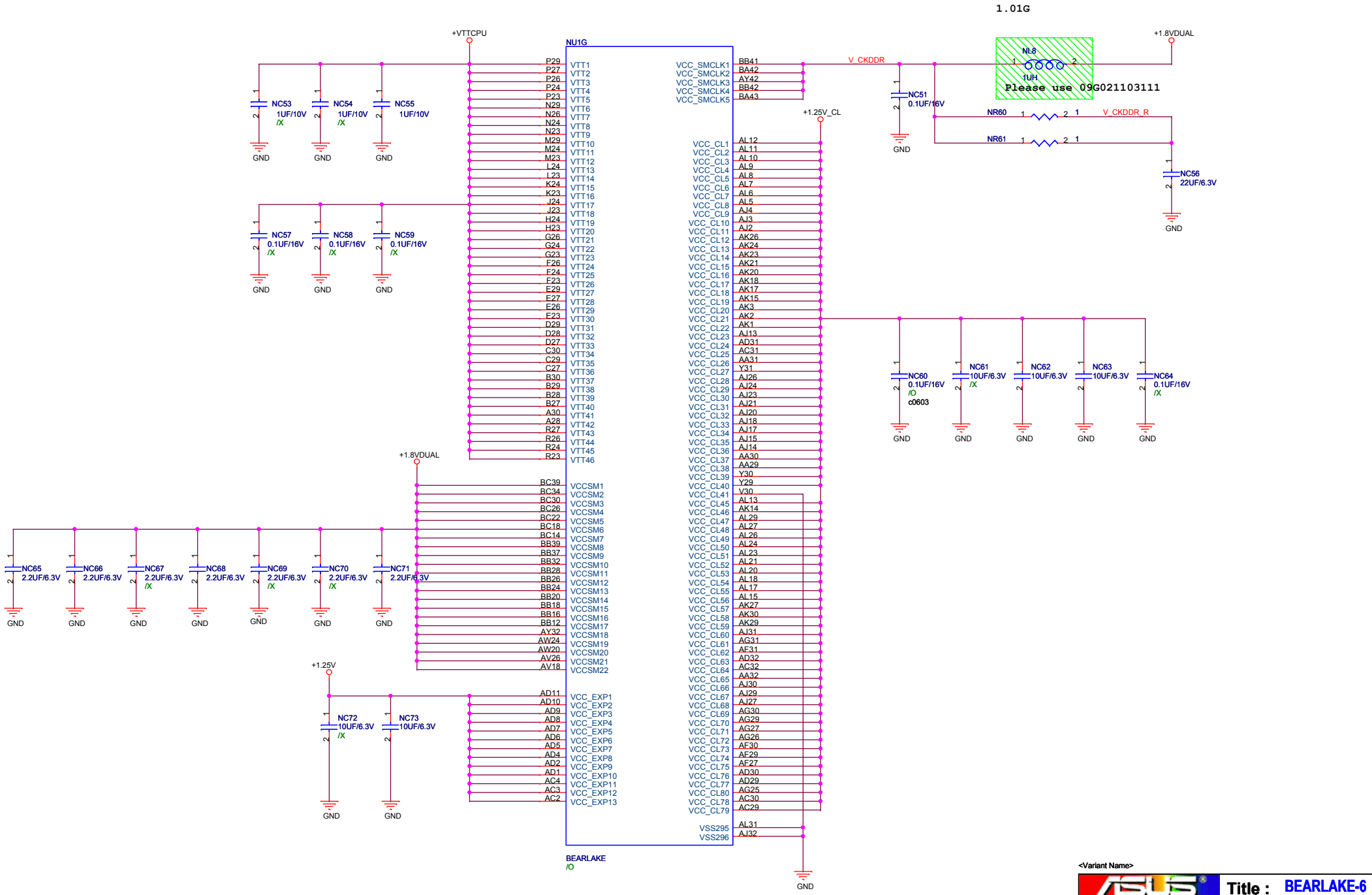
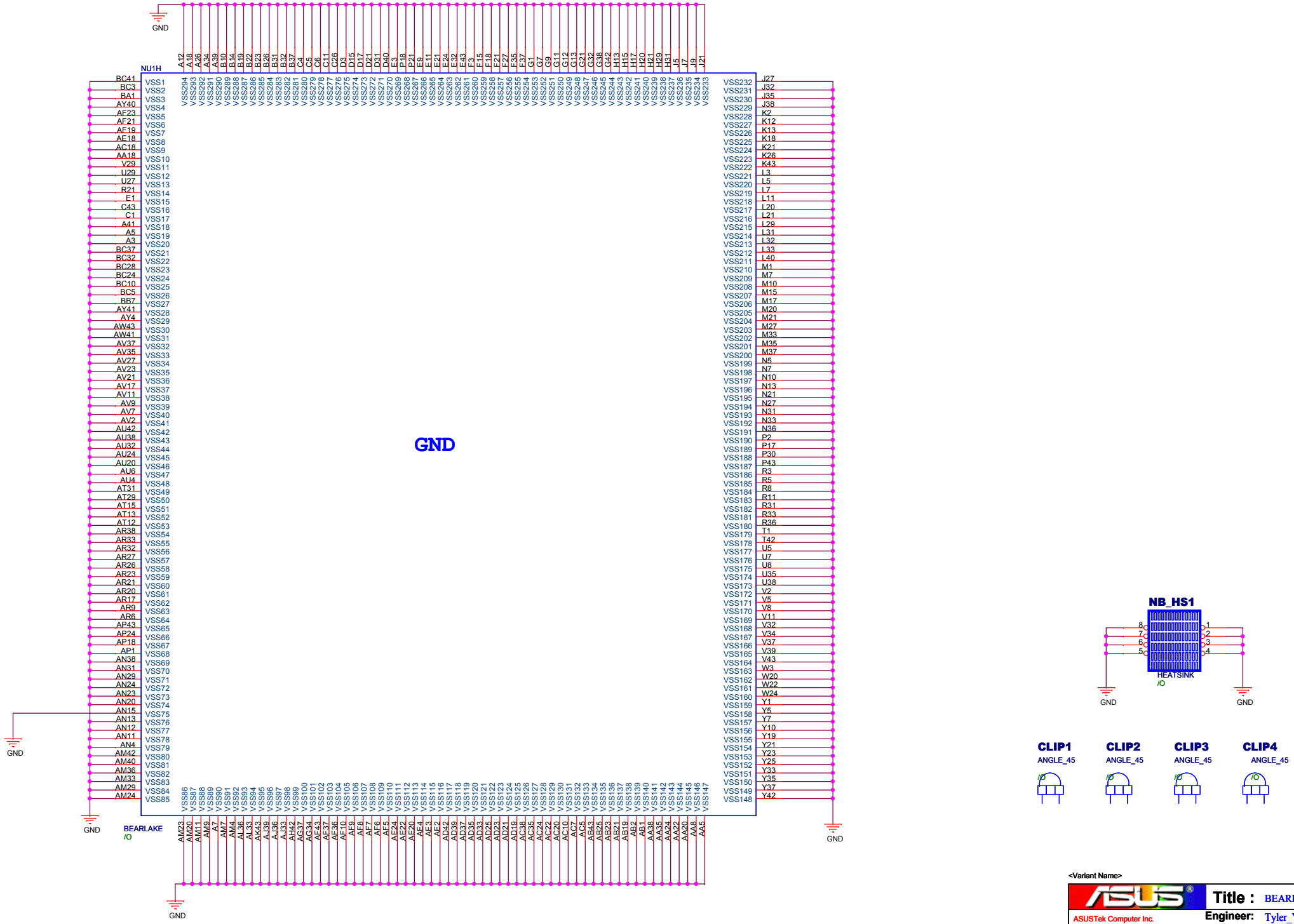
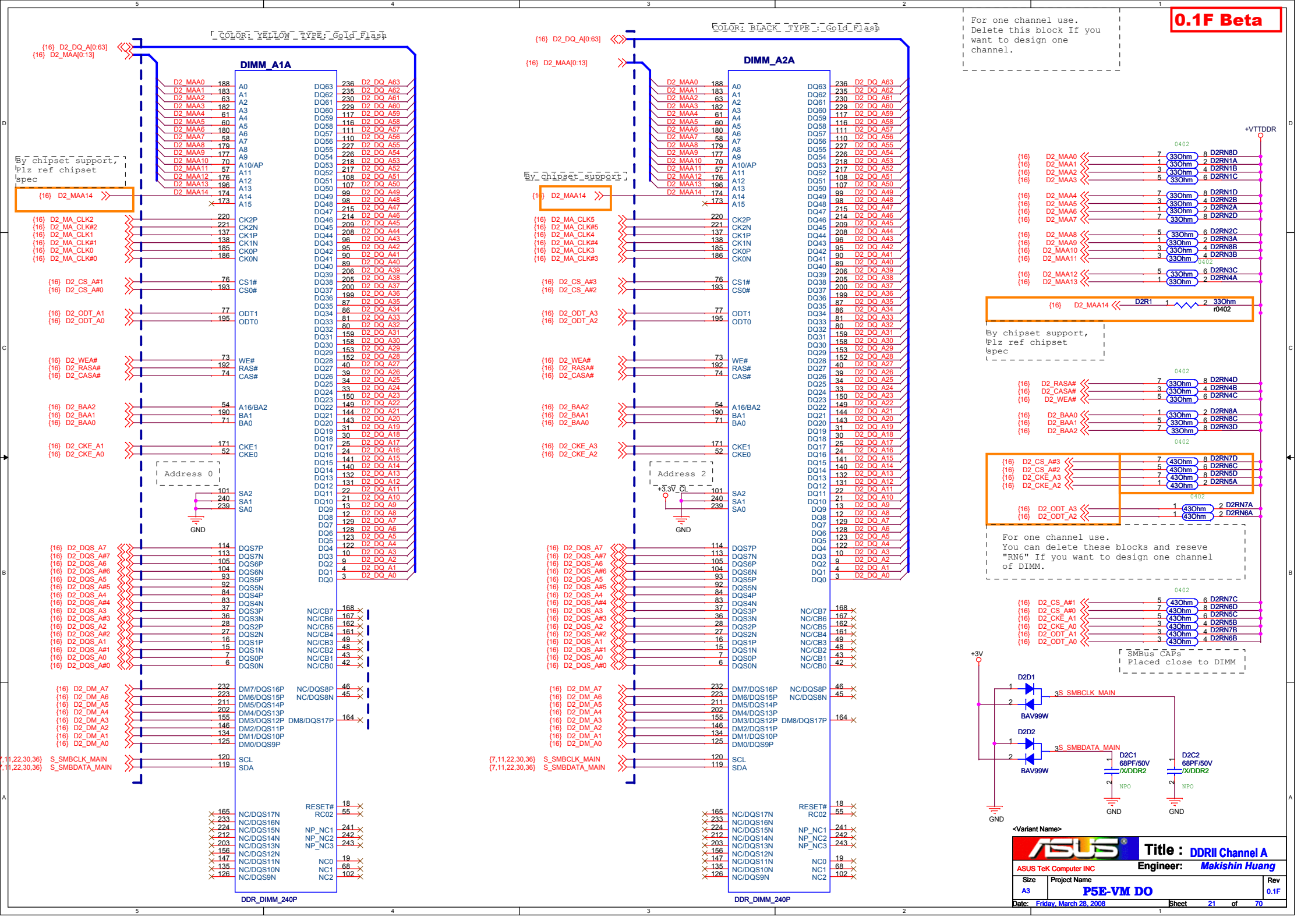
VCC_160
VCC_161
VCC_162
VCC_163
VCC_164
VCC_165
VCC_166
VCC_167
VCC_168
VCC_169
NC21
1UF/16V
NC18
1UF/16V
NC19
1UF/16V
NC20
1UF/16V
/X
NC27
22UF/6.3V
/X
c0805
NC29
1UF/10V
c0603
/O
NC30
1UF/10V
c0603
/O
NC31
1UF/10V
c0603
/O
NC32
1UF/10V
c0603
/X
NC34
4.7UF/6.3V
/X
NC43
2.2UF/6.3V
/O
c0603
NC44
2.2UF/6.3V
/X
c0603
<Variant Name>
Title : BEARLAKE-5
ASUSTek Computer Inc.
Engineer: Tyler_Yuan
Size A3
Project Name P5E-VM DO
Rev 1.01G
Date: Friday, March 28, 2008
Sheet 18 of 70

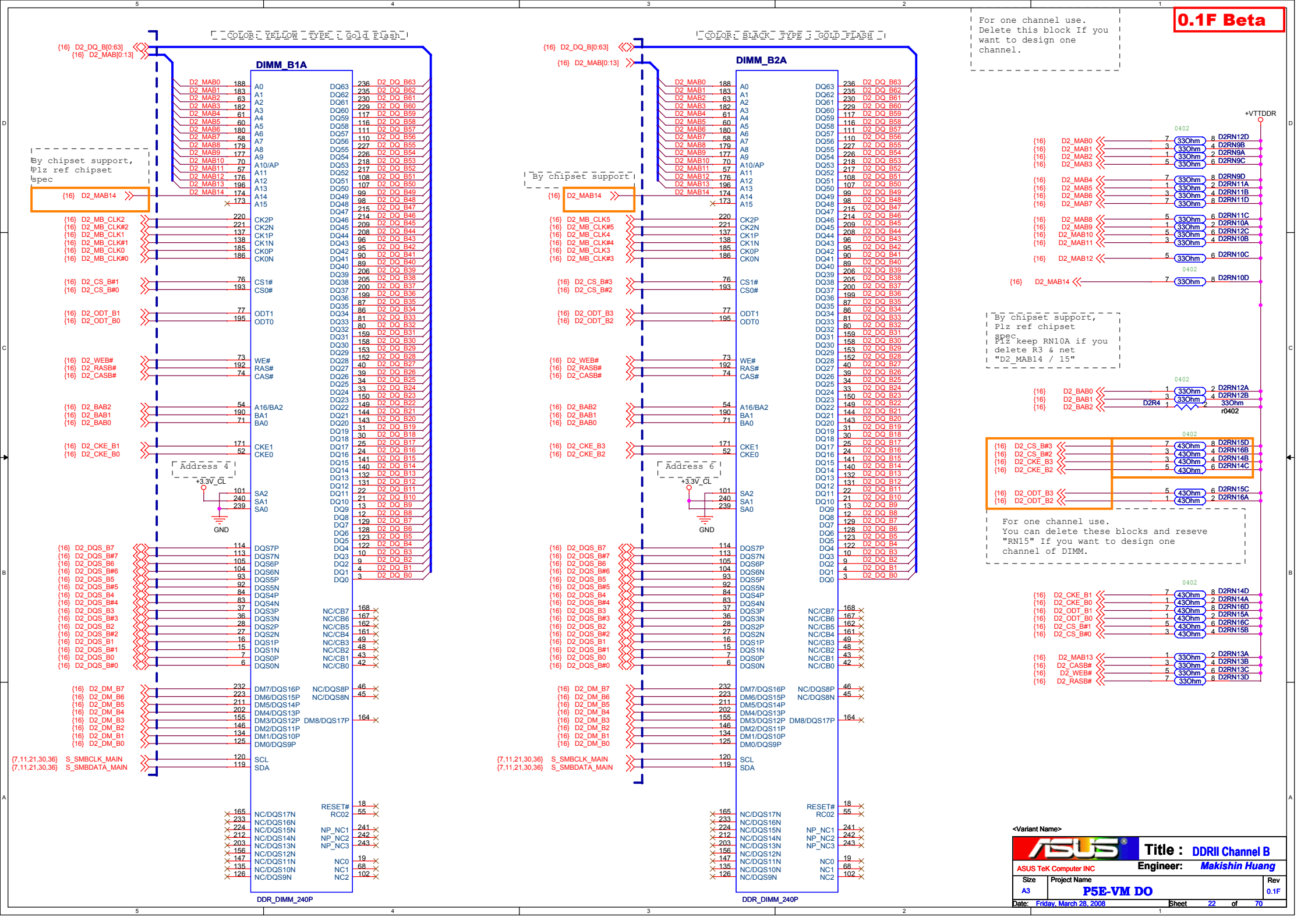

1.01G
+VTTCPU
NU1G
NC53 1UF/10V /X
NC54 1UF/10V /X
NC55 1UF/10V
NC57 0.1UF/16V /X
NC58 0.1UF/16V /X
NC59 0.1UF/16V /X
GND
P29 P27 P26 P24 P23 N29 N26 N24 N23 M29 M24 M23 L24 L23 K24 K23 J24 J23 H24 H23 G26 G24 G23 F26 F24 F23 E29 E27 E26 E23 D29 D28 D27 C30 C29 C27 B30 B29 B28 B27 A30 A28 R27 R26 R24 R23
VTT1 VTT2 VTT3 VTT4 VTT5 VTT6 VTT7 VTT8 VTT9 VTT10 VTT11 VTT12 VTT13 VTT14 VTT15 VTT16 VTT17 VTT18 VTT19 VTT20 VTT21 VTT22 VTT23 VTT24 VTT25 VTT26 VTT27 VTT28 VTT29 VTT30 VTT31 VTT32 VTT33 VTT34 VTT35 VTT36 VTT37 VTT38 VTT39 VTT40 VTT41 VTT42 VTT43 VTT44 VTT45 VTT46
VCC_SMCLK1 VCC_SMCLK2 VCC_SMCLK3 VCC_SMCLK4 VCC_SMCLK5
BB41 BA42 AY42 BB42 BA43
V_CKDDR
NC51 0.1UF/16V
NL8 1UH
Please use 09G021103111
+1.8VDUAL
NR60 V_CKDDR_R
NR61
NC56 22UF/6.3V
+1.25V_CL
VCC_CL1 VCC_CL2 VCC_CL3 VCC_CL4 VCC_CL5 VCC_CL6 VCC_CL7 VCC_CL8 VCC_CL9 VCC_CL10 VCC_CL11 VCC_CL12 VCC_CL13 VCC_CL14 VCC_CL15 VCC_CL16 VCC_CL17 VCC_CL18 VCC_CL19 VCC_CL20 VCC_CL21 VCC_CL22 VCC_CL23 VCC_CL24 VCC_CL25 VCC_CL26 VCC_CL27 VCC_CL28 VCC_CL29 VCC_CL30 VCC_CL31 VCC_CL32 VCC_CL33 VCC_CL34 VCC_CL35 VCC_CL36 VCC_CL37 VCC_CL38 VCC_CL39 VCC_CL40 VCC_CL41 VCC_CL45 VCC_CL46 VCC_CL47 VCC_CL48 VCC_CL49 VCC_CL50 VCC_CL51 VCC_CL52 VCC_CL53 VCC_CL54 VCC_CL55 VCC_CL56 VCC_CL57 VCC_CL58 VCC_CL59 VCC_CL60 VCC_CL61 VCC_CL62 VCC_CL63 VCC_CL64 VCC_CL65 VCC_CL66 VCC_CL67 VCC_CL68 VCC_CL69 VCC_CL70 VCC_CL71 VCC_CL72 VCC_CL73 VCC_CL74 VCC_CL75 VCC_CL76 VCC_CL77 VCC_CL80 VCC_CL78 VCC_CL79
AL12 AL11 AL10 AL9 AL8 AL7 AL6 AL5 AJ4 AJ3 AJ2 AK26 AK24 AK23 AK21 AK20 AK18 AK17 AK15 AK3 AK2 AK1 AJ13 AD31 AC31 AA31 Y31 AJ26 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AJ15 AJ14 AA30 AA29 Y30 Y29 V30 AL13 AK14 AL29 AL27 AL26 AL24 AL23 AL21 AL20 AL18 AL17 AL15 AK27 AK30 AK29 AJ31 AG31 AF31 AD32 AC32 AA32 AJ30 AJ29 AJ27 AG30 AG29 AG27 AG26 AF30 AF29 AF27 AD30 AD29 AG25 AC30 AC29
VSS295 VSS296
AL31 AJ32
NC60 0.1UF/16V /O c0603
NC61 10UF/6.3V /X
NC62 10UF/6.3V
NC63 10UF/6.3V
NC64 0.1UF/16V /X
+1.8VDUAL
BC39 BC34 BC30 BC26 BC22 BC18 BC14 BB39 BB37 BB32 BB28 BB26 BB24 BB20 BB18 BB16 BB12 AY32 AW24 AW20 AV26 AV18
VCCSM1 VCCSM2 VCCSM3 VCCSM4 VCCSM5 VCCSM6 VCCSM7 VCCSM8 VCCSM9 VCCSM10 VCCSM11 VCCSM12 VCCSM13 VCCSM14 VCCSM15 VCCSM16 VCCSM17 VCCSM18 VCCSM19 VCCSM20 VCCSM21 VCCSM22
NC65 2.2UF/6.3V
NC66 2.2UF/6.3V
NC67 2.2UF/6.3V /X
NC68 2.2UF/6.3V
NC69 2.2UF/6.3V /X
NC70 2.2UF/6.3V /X
NC71 2.2UF/6.3V
+1.25V
AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD2 AD1 AC4 AC3 AC2
VCC_EXP1 VCC_EXP2 VCC_EXP3 VCC_EXP4 VCC_EXP5 VCC_EXP6 VCC_EXP7 VCC_EXP8 VCC_EXP9 VCC_EXP10 VCC_EXP11 VCC_EXP12 VCC_EXP13
NC72 10UF/6.3V /X
NC73 10UF/6.3V
BEARLAKE
/O
<Variant Name>
Title : BEARLAKE-6
ASUSTek Computer Inc.
Engineer: Tyler_Yuan
Size A3
Project Name P5E-VM DO
Rev 1.01G
Date: Friday, March 28, 2008
Sheet 19 of 70

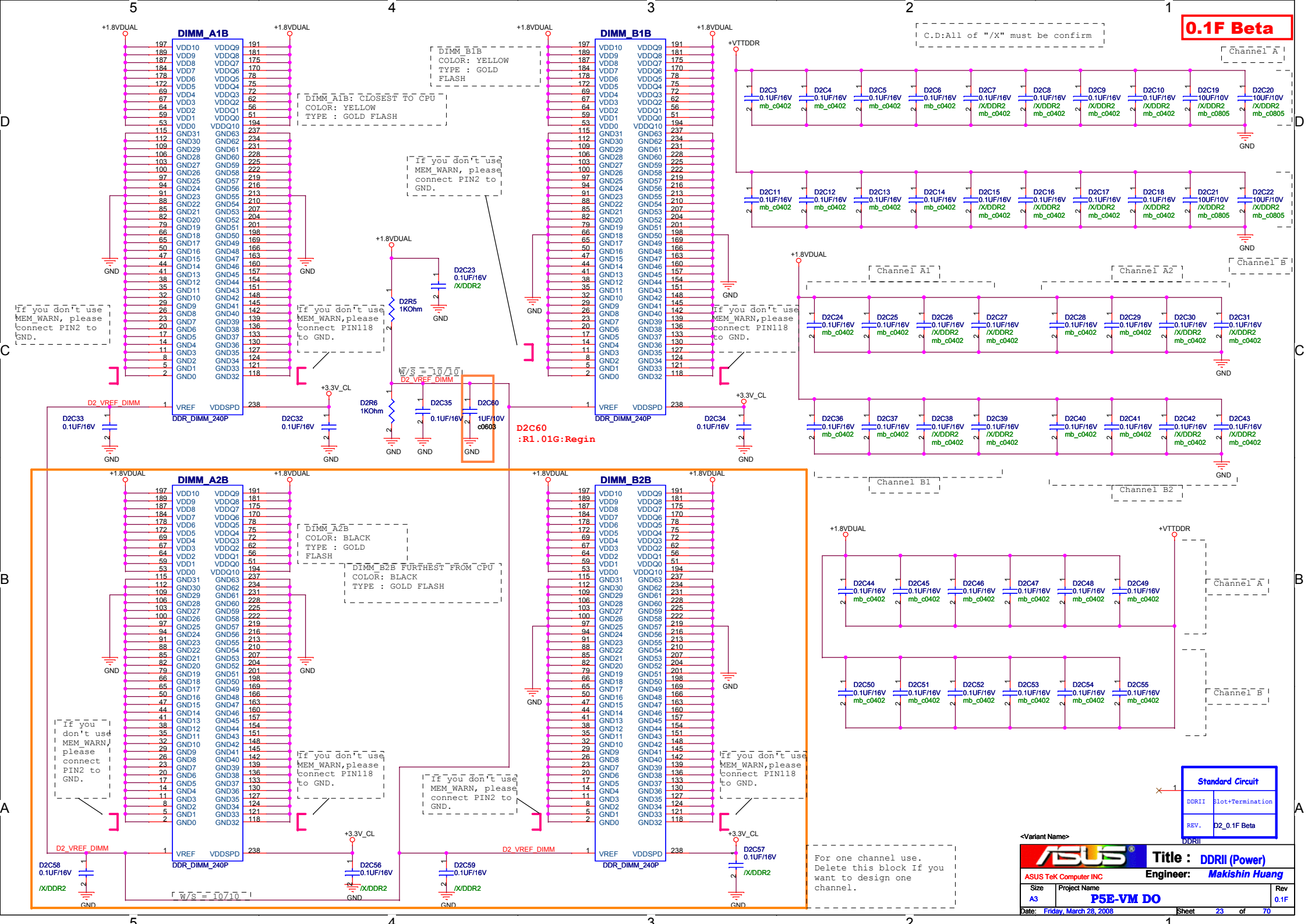


<Variant Name>

ASUSTek Computer Inc.	Title : BEARLAKE-7	
	Engineer: Tyler_Yuan	
Size: A3	Project Name: P5E-VM DO	Rev: 1.01G
Date: Friday, March 28, 2008	Sheet 20 of 70	


0.1F Beta
COLOR: YELLOW TYPE: Gold Flash
DIMM_A1A
COLOR: BLACK TYPE : Gold Flash
DIMM_A2A
For one channel use.
Delete this block If you want to design one channel.
By chipset support, Plz ref chipset spec
Address 0
Address 2
+3.3V_CL
GND
DDR_DIMM_240P
+VTTDDR
+3V
For one channel use.
You can delete these blocks and reseve "RN6" If you want to design one channel of DIMM.
SMBus CAPs Placed close to DIMM
D2D1
D2D2
BAV99W
D2C1
D2C2
68PF/50V
/X/DDR2
NPO
<Variant Name>
ASUS TeK Computer INC
Title : DDRII Channel A
Engineer: Makishin Huang
Size A3
Project Name P5E-VM DO
Rev 0.1F
Date: Friday, March 28, 2008
Sheet 21 of 70


COLOR: YELLOW TYPE : Gold Flash
DIMM_B1A
{16} D2_DQ_B[63:0]
{16} D2_MAB[0:13]
By chipset support, Plz ref chipset spec
{16} D2_MAB14
Address 4
+3.3V_CL
GND
DDR_DIMM_240P
COLOR: BLACK TYPE : GOLD FLASH
DIMM_B2A
By chipset support
Address 6
DDR_DIMM_240P
For one channel use. Delete this block If you want to design one channel.
0.1F Beta
+VTTDDR
By chipset support, Plz ref chipset spec
Plz keep RN10A if you delete R3 & net "D2_MAB14 / 15"
For one channel use. You can delete these blocks and reseve "RN15" If you want to design one channel of DIMM.
<Variant Name>
Title : DDRII Channel B
ASUS TeK Computer INC
Engineer: Makishin Huang
Size A3
Project Name P5E-VM DO
Rev 0.1F
Date: Friday, March 28, 2008
Sheet 22 of 70


0.1F Beta
C.D:All of "/X" must be confirm
DIMM_A1B
DIMM_B1B
DIMM_A2B
DIMM_B2B
DDR_DIMM_240P
DIMM_A1B: CLOSEST TO CPU
COLOR: YELLOW
TYPE : GOLD FLASH
DIMM_B1B
COLOR: YELLOW
TYPE : GOLD
FLASH
DIMM_A2B
COLOR: BLACK
TYPE : GOLD
FLASH
DIMM_B2B FURTHEST FROM CPU
COLOR: BLACK
TYPE : GOLD FLASH
If you don't use MEM_WARN, please connect PIN2 to GND.
If you don't use MEM_WARN,please connect PIN118 to GND.
W/S = 10/10
D2_VREF_DIMM
D2C60
:R1.01G:Regin
Channel A
Channel B
Channel A1
Channel A2
Channel B1
Channel B2
For one channel use. Delete this block If you want to design one channel.
Standard Circuit
DDRII Slot+Termination
REV. D2_0.1F Beta
DDRII
<Variant Name>
Title : DDRII (Power)
ASUS TeK Computer INC
Engineer: Makishin Huang
Size A3
Project Name P5E-VM DO
Rev 0.1F
Date: Friday, March 28, 2008
Sheet 23 of 70

For Intel Bearlake Chipset

0.2A Beta

Standard Circuit	
VGA	BEARLAKE
REV.	V_0.2A BETA

VGA_BEARLAKE
/X/VGA

Place near connector side

Place near NB side

+3V

VD1 BAV99W /VGA
VD3 BAV99W /VGA
VD4 BAV99W /VGA

VC2 0.1UF/16V mb_c0402 /X/VGA

+V_5V_L — VL4 70Ohm/100Mhz mb_l0805 — +V_5V_F — VF1 1.1A/8V — +V_5V — VD2 SS14 — +5V

VC15 0.1UF/16V mb_c0402

{17} V_RED
{17} V_GREEN
{17} V_BLUE

VLX1 0.082uH
VLX2 0.082uH
VLX3 0.082uH

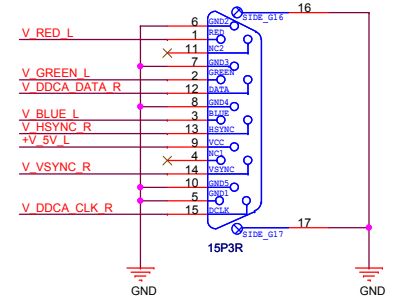
V_RED_L
V_GREEN_L
V_BLUE_L

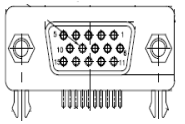
VC30 10PF/50V NPO /X/VGA
VC31 10PF/50V NPO /X/VGA
VC32 10PF/50V NPO /X/VGA
VR12 150Ohm mb_r0402 1%
VR13 150Ohm mb_r0402 1%
VR14 150Ohm mb_r0402 1%
VR15 150Ohm mb_r0402 1%
VR16 150Ohm mb_r0402 1%
VR17 150Ohm mb_r0402 1%
VC16 10PF/50V NPO
VC17 10PF/50V NPO
VC18 10PF/50V NPO
VC19 27PF/50V NPO
VC20 27PF/50V NPO
VC21 27PF/50V NPO

GND

Right Angle (Default)

VGA





+3V

VR34 2.7KOhm
VR35 2.7KOhm

+V_5V

VR31 2.7KOhm
VR30 2.7KOhm

{17} V_DDCA_DATA
{17} V_DDCA_CLK

VQ6 H2N7002
VQ7 H2N7002

V_DDCA_DATA_Q
V_DDCA_CLK_Q

VR18 100Ohm
VR19 100Ohm

VD5 BAV99W /X/VGA
VD6 BAV99W /X/VGA

V_DDCA_DATA_R
V_DDCA_CLK_R

VC22 100PF/50V /X/VGA NPO
VC23 100PF/50V /X/VGA NPO

mb_r0402 VR32 0Ohm
mb_r0402 VR33 0Ohm

+5V

{17} V_HSYNC
{17} V_VSYNC

VU1A SN74HCT125DR /X/VGA
VU1D SN74HCT125DR /X/VGA

V_HSYNC_U
V_VSYNC_U

VRX1 33Ohm
VRX2 33Ohm

V_HSYNC_R
V_VSYNC_R

VC27 100PF/50V /X/VGA NPO
VC26 100PF/50V /X/VGA NPO
VC34 0.1UF/16V mb_c0402

VU1B SN74HCT125DR /X/VGA
VU1C SN74HCT125DR /X/VGA

<Variant Name>

ASUSTek Computer Inc.

Title : Onboard VGA(BL)

Engineer: C.W. Huang

Size	Project Name	Rev
A3	P5E-VM DO	0.2A

Date: Friday, March 28, 2008 Sheet 24 of 70

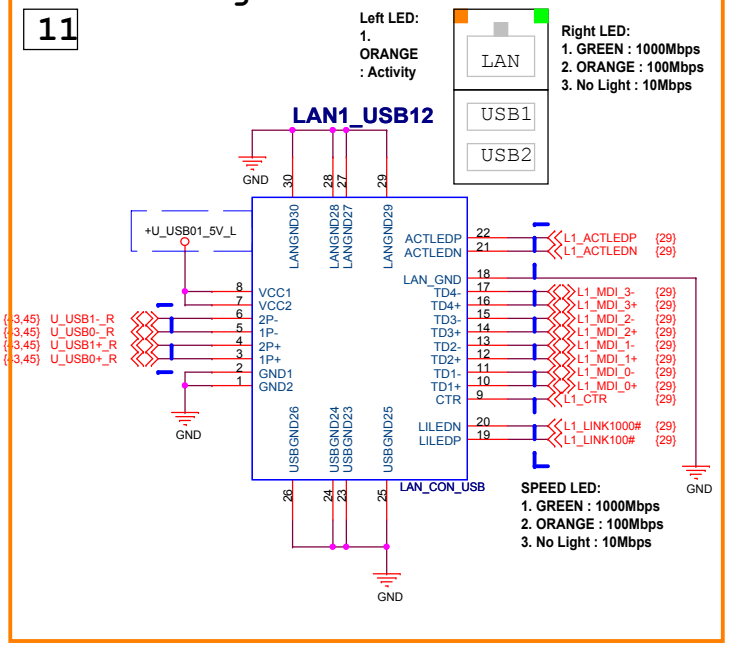
0.2A Beta

1.For single GIGA LAN1

11

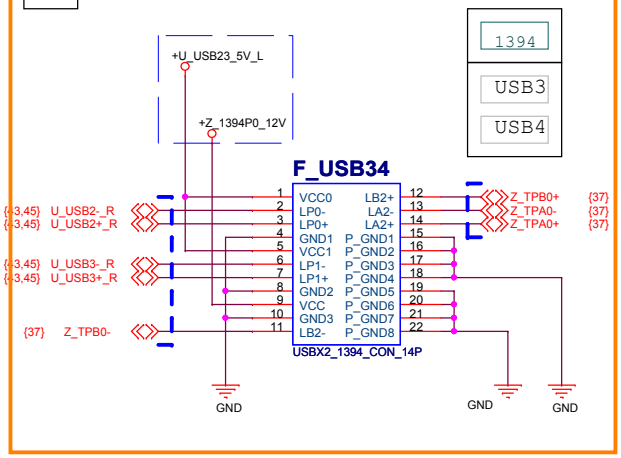
Left LED:
1.
ORANGE
: Activity

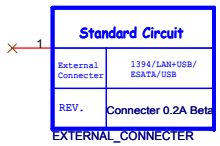
Right LED:
1. GREEN : 1000Mbps
2. ORANGE : 100Mbps
3. No Light : 10Mbps

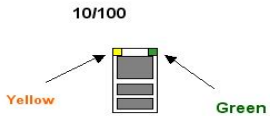


SPEED LED:
1. GREEN : 1000Mbps
2. ORANGE : 100Mbps
3. No Light : 10Mbps

5







Lan chip	Yellow (Left)	Green (Right)
Phy Realtek RTL8201 series	100M Activity	10M Activity
Phy VIA VT6103 series	On: 100M Link Off: 10M Link	Activity
Recommanded design	Activity	On: 100M Link Off: 10M Link

<Variant Name>

ASUSTEK Computer INC

Title : Connector2

Engineer: Makishin_Huang

Size	Project Name	Rev
A3	P5E-VM DO	0.2A

Date: Friday, March 28, 2008 Sheet 25 of 70

PCIEX16_1

若無使用SLOT_WARN線路,
請將X_1X16_DET_A接至GND.

X_WAKE#需在SB端Pull-high

(1)
如有使用,需在SB端以8.2K OhmPull high至+3V.

(2)
若不使用,請RD將其接至GND,不能floating,並請確認SB是否需要Pull high or pull down.

(3)
若Chipset有support SDVO,請RD自行修改Netname.沒有使用的Net請接至GND,不能floating.

若無使用SLOT_WARN線路,
請將X_1X16_DET_[A:B]接至GND.

Default :Blue,G/F,Latch往上
若要使用15U的SLOT,
請RD自行更換
料號：12V306164UU2

Standard Circuit

PCIEX	PCIEX_SLOT
REV.	X_0.1F Beta

PCIEX_SLOT /X/PCIE

PCI_EXPRESS_X16

<variant_name>

ASUSTek Computer Inc.

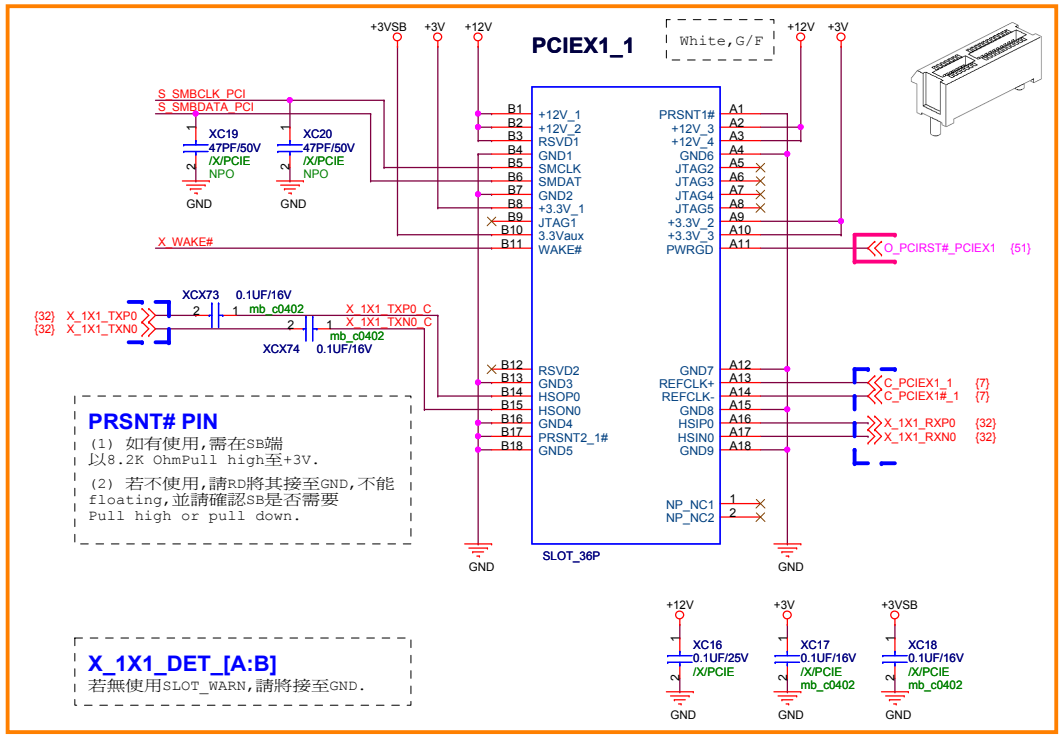
Title : PCIEX16_1

Engineer: Eddie Chiu

Size	Project Name	Rev
A3	P5E-VM DO	0.1F

Date: Friday, March 28, 2008 Sheet 26 of 70

0.2A Beta



S_SMBCLK_PCI & S_SMBDATA_PCI

需接至SB SMBus(吃standby power)

{26,28,34,36} S_SMBCLK_PCI
{26,28,34,36} S_SMBDATA_PCI
{26,34} X_WAKE#

X_WAKE#

需在SB端Pull-high

<Variant Name>

ASUSTek Computer Inc.

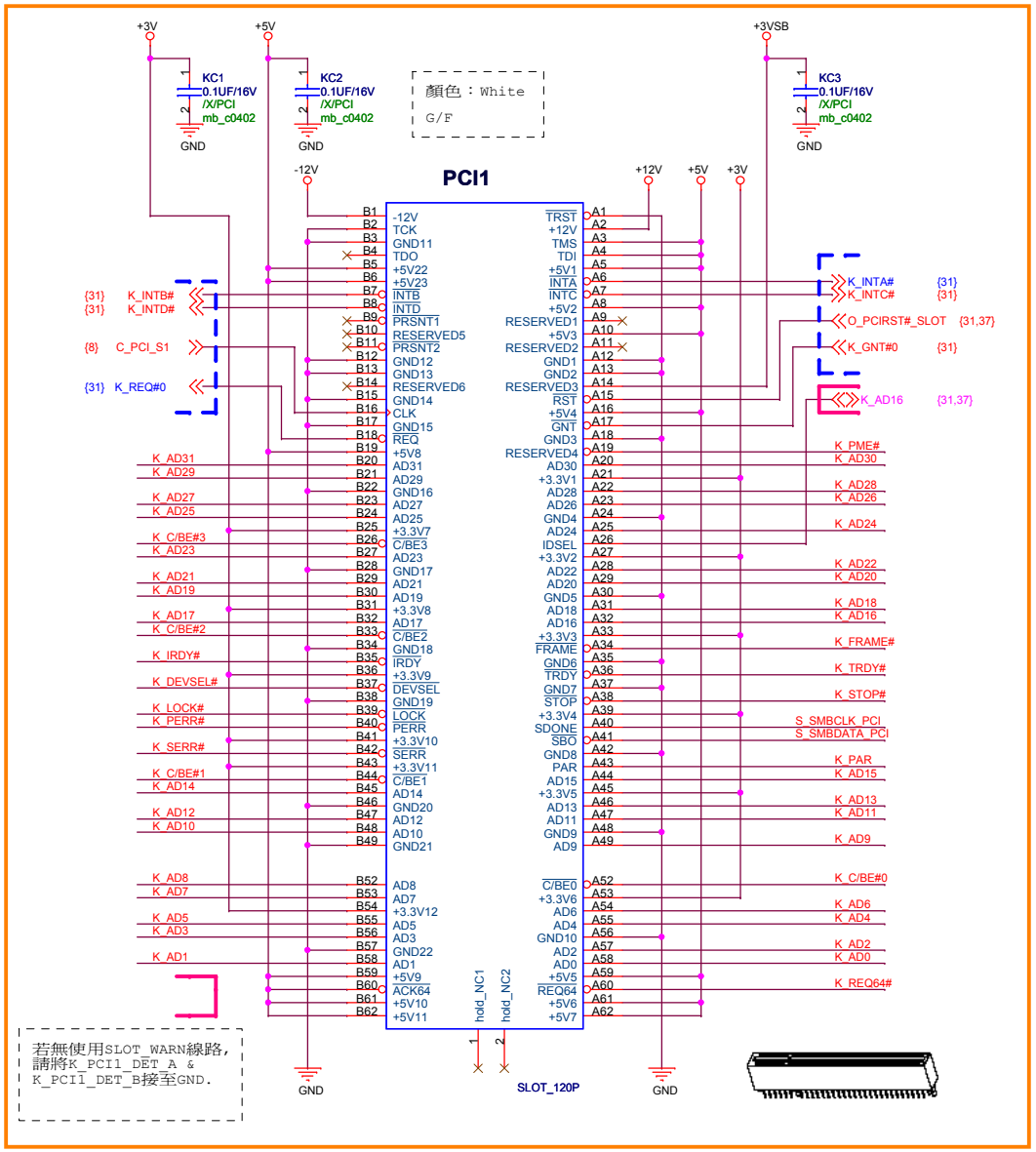
Title : PCIEX1_1

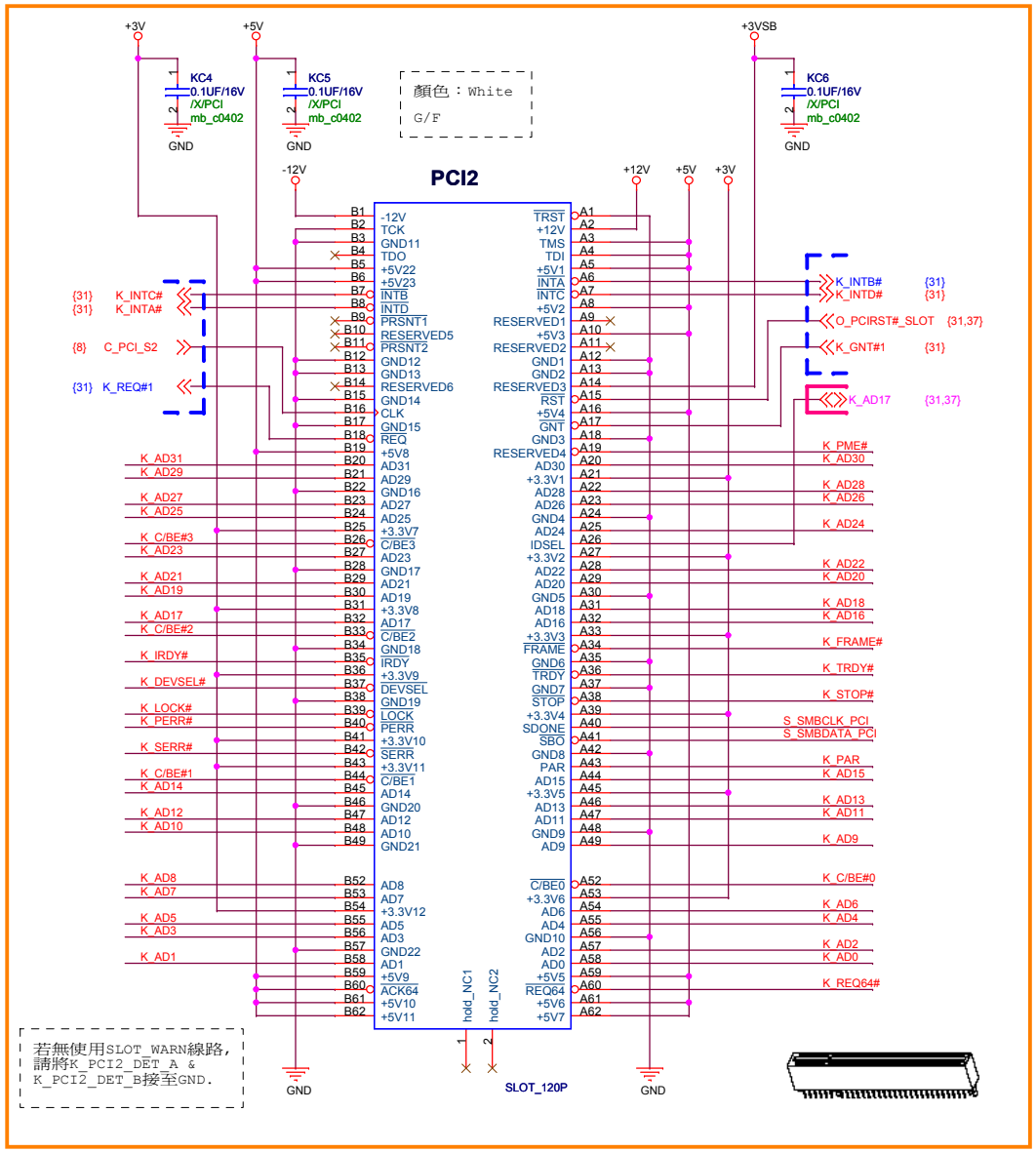
Engineer: Eddie Chiu

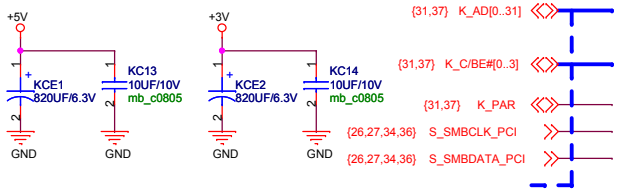
Size	Project Name	Rev
A3	P5E-VM DO	0.2A

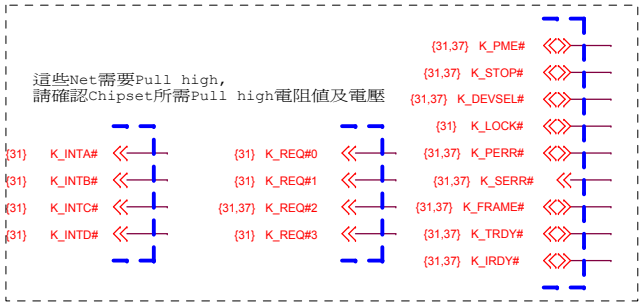
Date: Friday, March 28, 2008 Sheet 27 of 70

0.1E Beta









K_REQ64# 爲PCI slot useonly,需要8.2K Pull high to +5V,電阻可與其他net合併使用

{31} K_REQ64#

Standard Circuit

PCI	PCI_SLOT
REV.	K_0.1E BETA

PCI_SLOT /X/PCI

PCI SLOT有兩個料號,分別對應長卡及短卡
請依PES所需之PCI SLOT種類做選擇 .（Default爲長卡）

料號及相對應的Footprint :
12V306120W00（長） -->mb_slot_pci_120p_long_lf3
12V306120W01（短） -->mb_slot_pci_120p_short_lf3

<Variant Name>

ASUSTek Computer Inc.

Title : PCI_SLOT-1

Engineer: Eddie Chiu

Size	Project Name	Rev
A3	P5E-VM DO	0.1E

Date: Friday, March 28, 2008 Sheet 28 of 70

0.2A Beta

ICH side

Place near PHY side

Place near ICH side

PERp6/GLAN_RXP
PERn6/GLAN_RXN
{32} L1_GLCI_TXP_PHY
{32} L1_GLCI_TXN_PHY
mb_c0402 L1CX1 0.1UF/16V
mb_c0402 L1CX2 0.1UF/16V
L1_GLCI_TXP_C H2
L1_GLCI_TXN_C I2
L1_GLCI_RXP_C I4
L1_GLCI_RXN_C H4

PETp6/GLAN_TXP
PETn6/GLAN_TXN
{32} L1_GLCI_RXP_PHY
{32} L1_GLCI_RXN_PHY
mb_c0402 L1CX3 0.1UF/16V
mb_c0402 L1CX4 0.1UF/16V

L1U1
GLAN_TXP
GLAN_TXN
GLAN_RXP
GLAN_RXN

LAN_RXD0
LAN_RXD1
LAN_RXD2
{31} L1_LCI_JRXD2
{31} L1_LCI_JRXD1
{31} L1_LCI_JRXD0
C1 JRXD2
D2 JRXD1
D3 JRXD0

LAN_TXD0
LAN_TXD1
LAN_TXD2
{31} L1_LCI_JTXD2
{31} L1_LCI_JTXD1
{31} L1_LCI_JTXD0
F1 JTXD2
F3 JTXD1
D1 JTXD0

GLAN_CLK
LAN_RSTSYNC
{31} L1_LCI_JKCLK
{31} L1_LCI_JRSTSYNC
L1R9 33Ohm
L1_LCI_JKCLK_R
E2 JKCLK
E3 JRSTSYNC

LAN_RST#
{31} L1_LAN_RST#
L1R18 15KOhm /82566-1 1%
+3.3V_CL
L1R10 1.4KOhm 1%
L1R11 1.4KOhm 1%
O_RSMRST#
{7,34,57}
L1_KBIAS_P
L1_KBIAS_N
L1_RBIAS_P
G7 KBIAS_P
H7 KBIAS_N
E7 RBIAS_P
E6 RBIAS_N
L1R19 0Ohm /X/82566-1
L1C27 2.2UF/6.3V /82566-1 c0603
LR3 0Ohm /X/82566-1
FOR NON AMT
GND

C3 CTRL_10

+L1_1.0VSB_INT
B1 V1P0_OUT
L1C11 10UF/10V mb_c0805
L1C12 0.1UF/16V mb_c0402
L1C13 0.1UF/16V mb_c0402
L1C14 0.1UF/16V mb_c0402
L1C15 0.1UF/16V mb_c0402 /X/82566-1
D7 VDD1P0_1
D4 VCC1
E4 VCC2
E8 VDD1P0_2
E5 VCCF1P0
G4 VCC1P0
F7 VDD1P0_3
H3 VCCFC1P0

+3.3V_CL
Place near transistor
L1R14 1.5Ohm mb_r1206
L1R15 1.5Ohm mb_r1206
Doc "82566_dc"
L1C16 10UF/10V mb_c0805
L1C17 0.1UF/16V mb_c0402
L1_+1.8VSB_CTRL_C
L1C20 0.01UF/50V
Intel Spec Update: Errata #5 solve Excess Noise on 1.8V Supply
L1Q1 BCP69-16
Parameters are critical. Use BCP69
07G003088211
07G003088112
L1_+1.8VSB_CTRL
B2 CTRL_18

+L1_1.8VSB
L1C21 10UF/10V mb_c0805
L1C22 1UF/6.3V mb_c0402 /X/82566-1
L1C23 0.1UF/16V mb_c0402
L1C24 0.1UF/16V mb_c0402
C2 VCC1P8_1
D5 VCC1P8_2
F5 VCC1P8_3
G5 VCC1P8_4

+3.3V_CL
L1C25 10UF/10V mb_c0805 /X/82566-1
L1C26 0.1UF/16V mb_c0402
F2 VCC3P3_1
B3 VCC3P3_2

NINEVEH

L1R1 49.9Ohm
L1R2 49.9Ohm
L1R3 49.9Ohm
L1R4 49.9Ohm
L1R5 49.9Ohm
L1R6 49.9Ohm
L1R7 49.9Ohm
L1R8 49.9Ohm
L1_ACTERMINATION0 L1C1 0.1UF/25V
L1_ACTERMINATION1 L1C2 0.1UF/25V
L1_ACTERMINATION2 L1C3 0.1UF/25V
L1_ACTERMINATION3 L1C4 0.1UF/25V
GND

MDI_MINUS[3] H9
MDI_PLUS[3] H8
MDI_MINUS[2] F8
MDI_PLUS[2] F9
MDI_MINUS[1] D8
MDI_PLUS[1] D9
MDI_MINUS[0] B9
MDI_PLUS[0] B8
L1_MDI_3- {25}
L1_MDI_3+ {25}
L1_MDI_2- {25}
L1_MDI_2+ {25}
L1_MDI_1- {25}
L1_MDI_1+ {25}
L1_MDI_0- {25}
L1_MDI_0+ {25}

L1RN1B 300Ohm
L1RN1C 300Ohm
XTAL1 H6 L1_XIN
XTAL2 H5 L1_XOUT
L1_XOUT_R
L1X1 25Mhz
L1R17 33Ohm
L1C5 33PF/50V /O NPO
L1C6 33PF/50V /O NPO
GND

+3.3V_CL
L1RN1D 300Ohm

LED0 A4
LED1 B4
LED2 A5
L1_LINK1000# R
L1RN1A 300Ohm
L1_ACTLEDP {25}
L1_ACTLEDN {25}
L1_LINK1000# {25}
L1_LINK100# {25}

TEST_EN B6 L1_TEST_EN
L1R13 100Ohm
GND

L1C7 /82566-1 1000PF/50V
L1C8 /82566-1 1000PF/50V
L1C9 /82566-1 1000PF/50V
L1C10 /82566-1 1000PF/50V
GND

RESERVED1 I6
RESERVED2 I7
RESERVED3 A6
RESERVED4 C5
RESERVED5 B5

IEEE_TEST_N B7 L1_IEEE_TEST_N
IEEE_TEST_P A7 L1_IEEE_TEST_P
L1R16 0Ohm /X/82566-1
Test 125MHz clock jitter

THERM_D_N A3
THERM_D_P A2

JTAG_TMS G2
JTAG_TDO G3
JTAG_TDI H1
JTAG_TCK G1

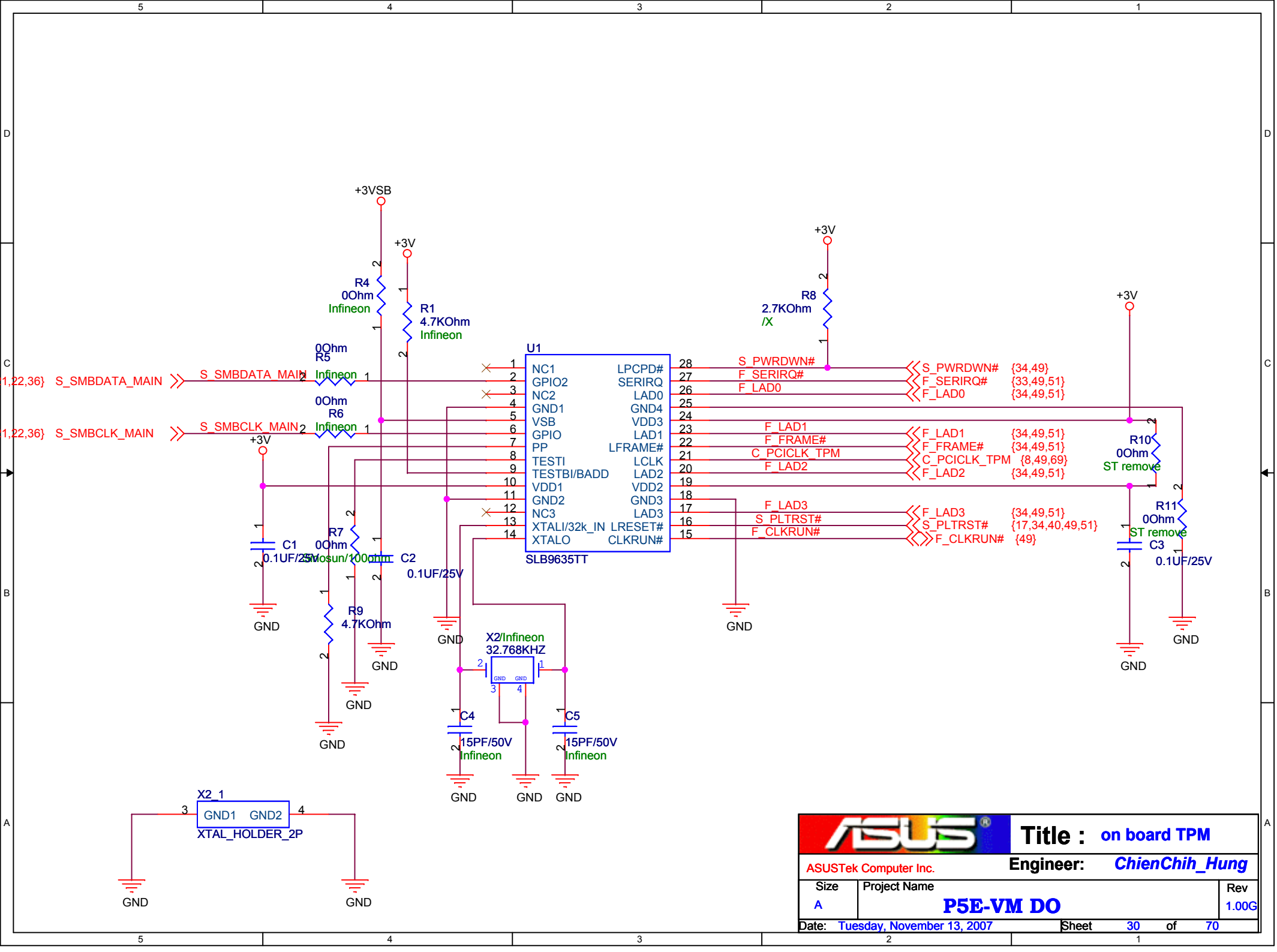
+L1_1.8VSB
L1L1 0Ohm
L1_CTR {25}
L1C19 0.1UF/16V mb_c0402 /82566-1
L1C18 0.1UF/16V mb_c0402
GND

VSS1 A1
VSS2 C4
VSS3 E1
VSS4 F4
VSSA1 I9
VSSA2 I8
VSSA3 I5
VSSA4 I3
VSSA5 I1
VSSA6 G9
VSSA7 G8
VSSA8 G6
VSSA9 F6
VSSA10 E9
VSSA11 D6
VSSA12 C9
VSSA13 C8
VSSA14 C7
VSSA15 C6
VSSA16 A9
VSSA17 A8
GND

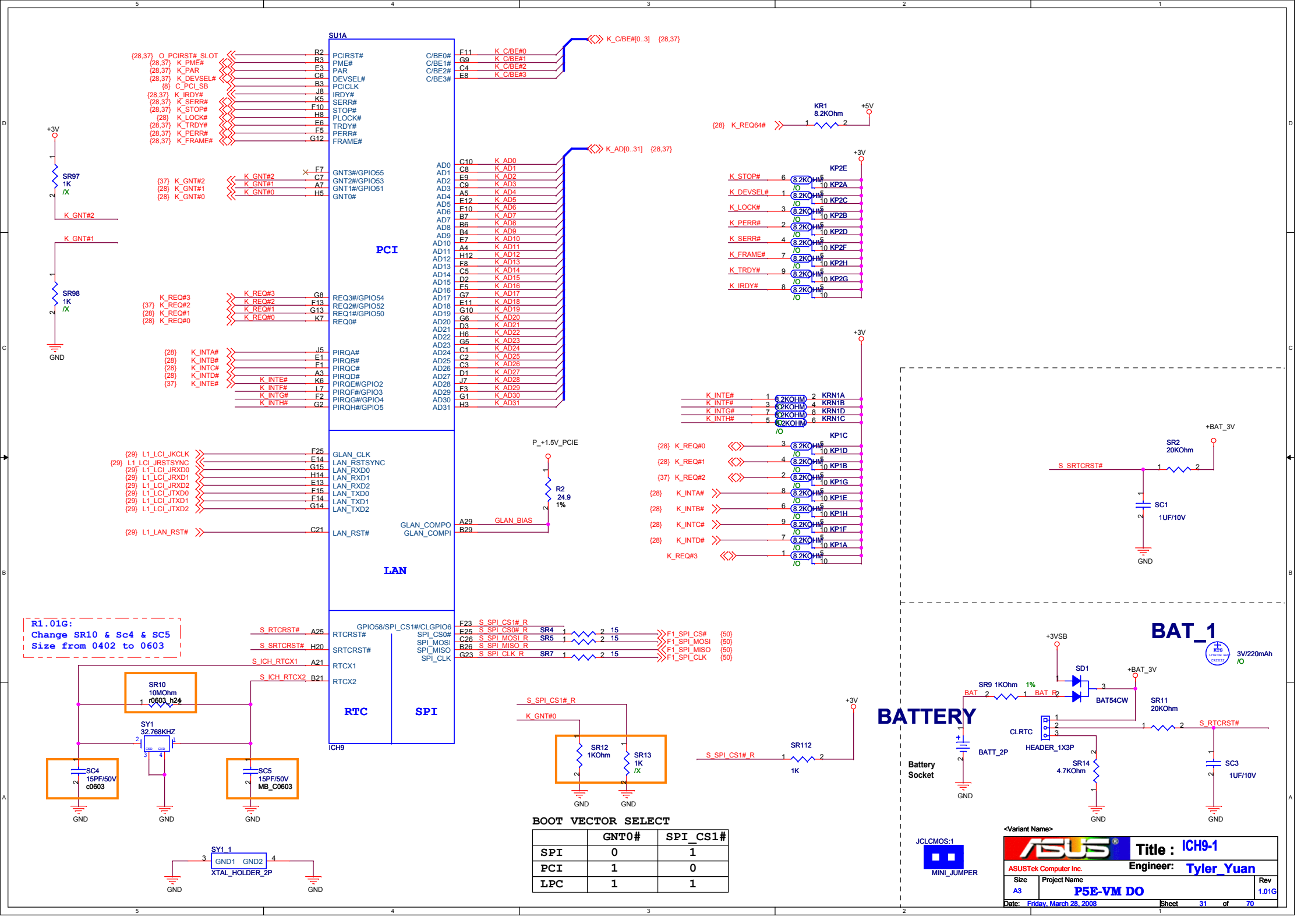
Standard Circuit
Intel PHY 82566DM
REV. L1_0.2A BETA
INTEL_82566DM
/X/82566-1

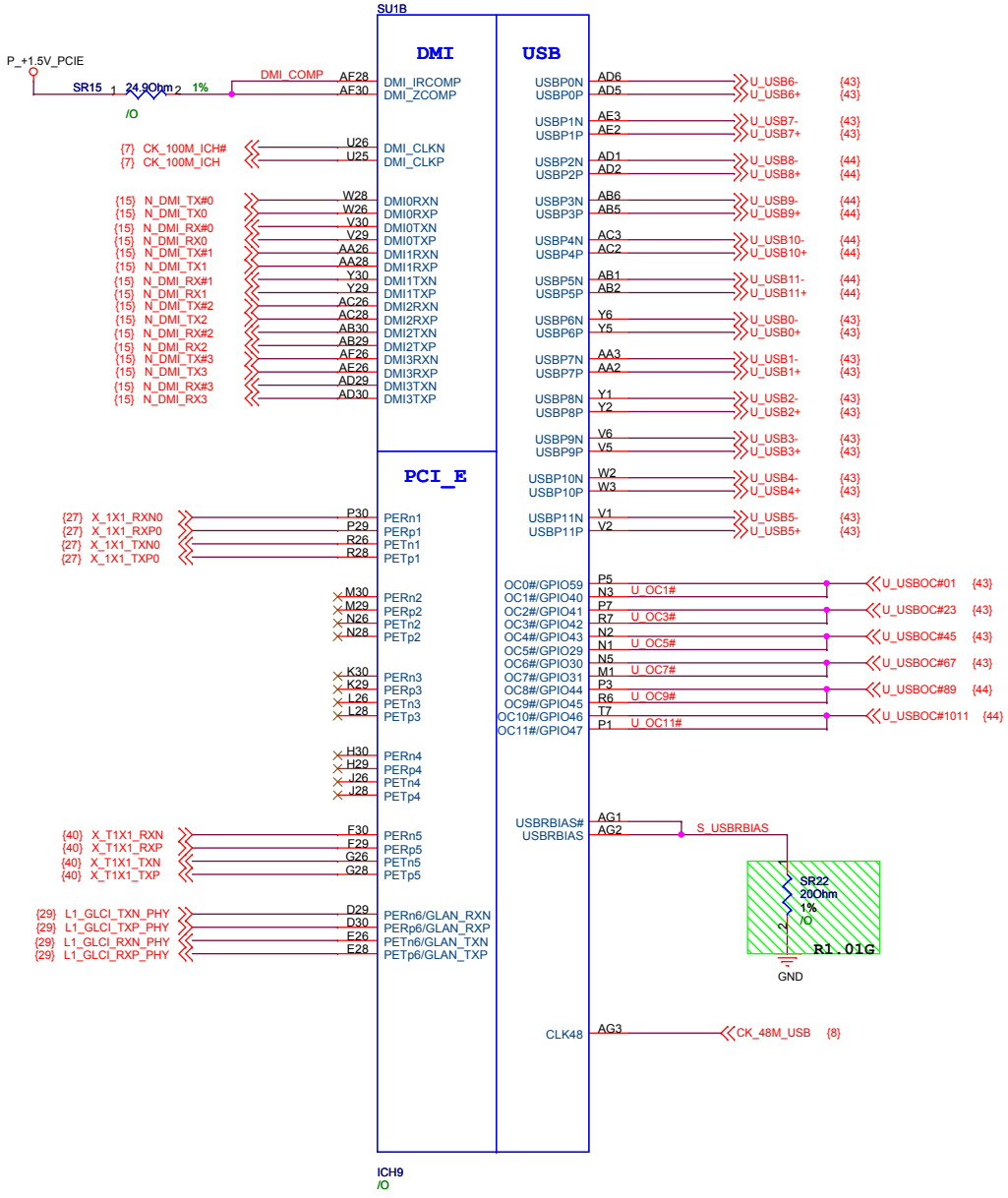
<Variant Name>

ASUSTek Computer Inc.
Title : L1 Intel 82566
Engineer: Nick Kao
Size A3
Project Name P5E-VM DO
Rev 0.1A
Date: Friday, March 28, 2008
Sheet 29 of 70



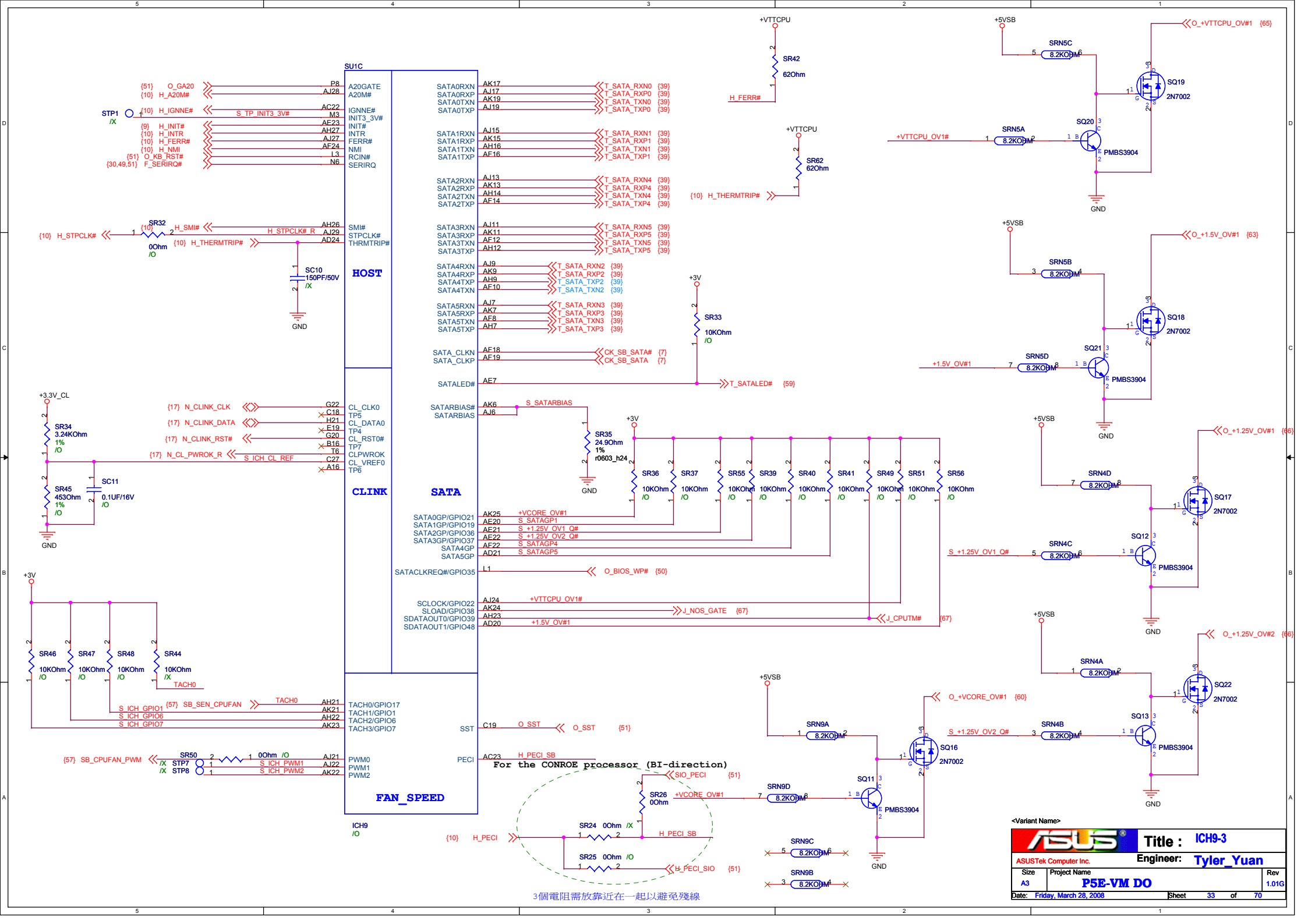
ASUSTek Computer Inc.	Title : on board TPM	
	Engineer: ChienChih_Hung	
Size: A	Project Name: P5E-VM DO	Rev: 1.00G
Date: Tuesday, November 13, 2007	Sheet 30 of 70	

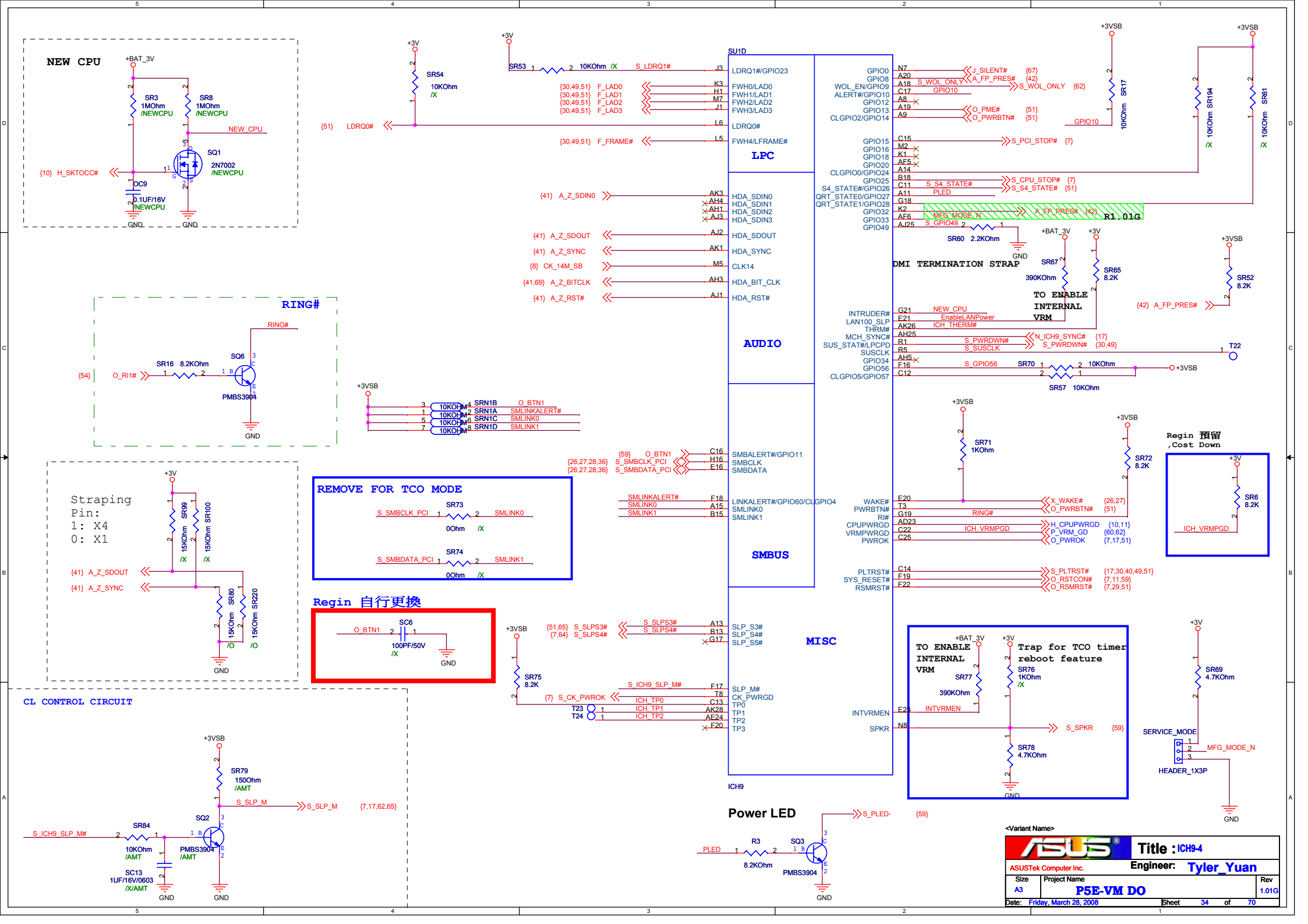

SU1A
PCI
LAN
RTC
SPI
ICH9
R1.01G:
Change SR10 & Sc4 & SC5
Size from 0402 to 0603
BOOT VECTOR SELECT
GNT0#
SPI_CS1#
SPI 0 1
PCI 1 0
LPC 1 1
BAT_1
BATTERY
Battery Socket
3V/220mAh
Title : ICH9-1
ASUSTek Computer Inc.
Engineer: Tyler_Yuan
Project Name P5E-VM DO
Rev 1.01G
Date: Friday, March 28, 2008
Sheet 31 of 70

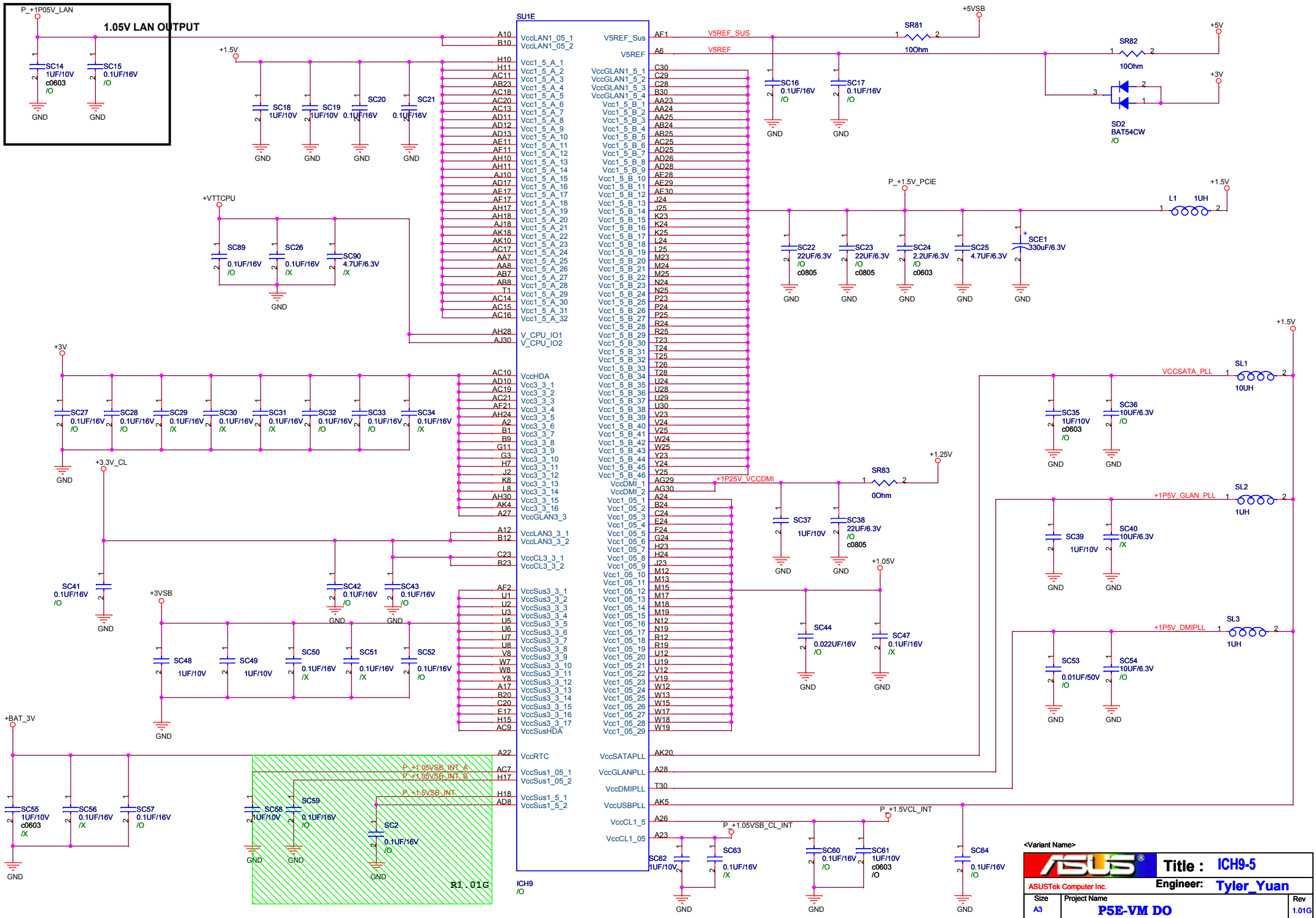


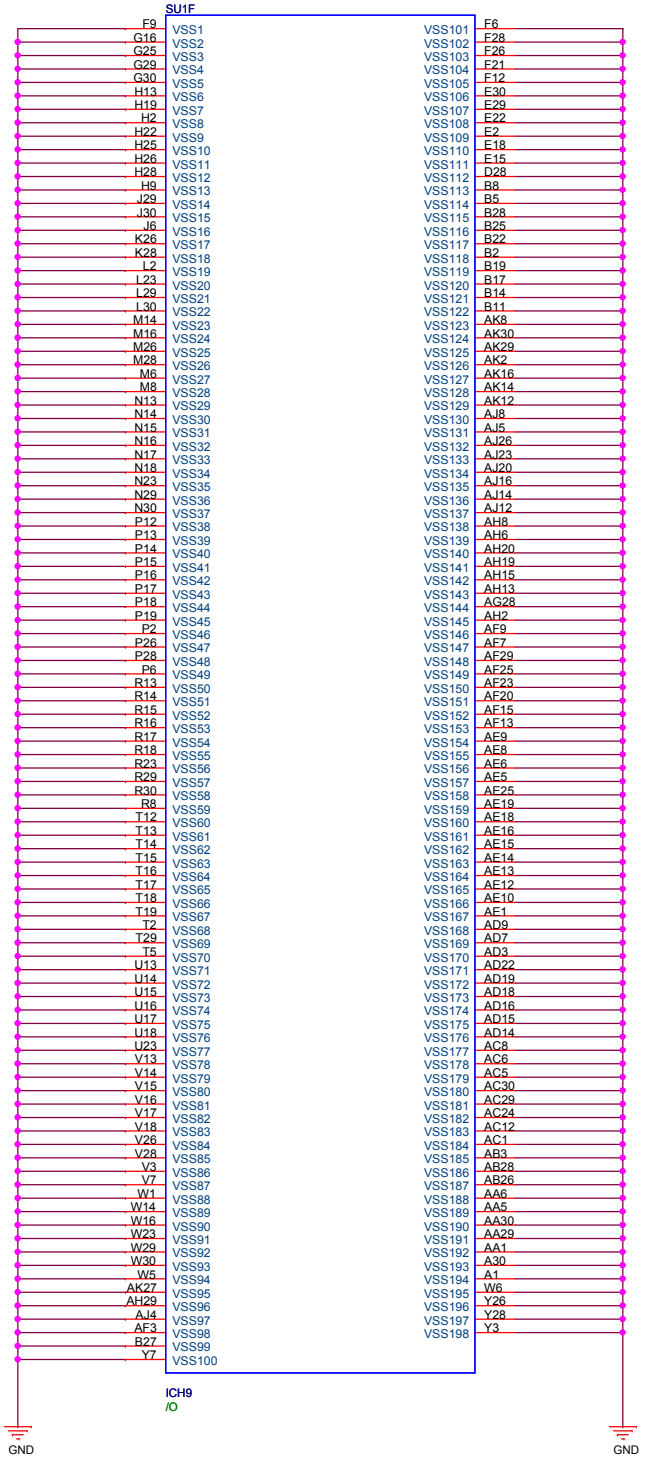
<Variant Name>

ASUSTek Computer Inc.	Title : ICH9-2	
	Engineer: Tyler_Yuan	
Size: A3	Project Name: P5E-VM DO	Rev: 1.00G
Date: Friday, March 28, 2008	Sheet 32 of 70	


SU1C
HOST
CLINK
SATA
FAN_SPEED
ICH9
/O
A20GATE
A20M#
IGNNE#
INIT3_3V#
INIT#
INTR
FERR#
NMI
RCIN#
SERIRQ
SMI#
STPCLK#
THRMTRIP#
CL_CLK0
CL_DATA0
CL_RST0#
CLPWROK
CL_VREF0
TACH0/GPIO17
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
PWM0
PWM1
PWM2
SST
PECI
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXP
SATA4TXN
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATALED#
SATARBIAS#
SATARBIAS
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
SATA4GP
SATA5GP
SATACLKREQ#/GPIO35
SCLOCK/GPIO22
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
STP1
/X
SR32
0Ohm
/O
SC10
150PF/50V
/X
SR34
3.24KOhm
1%
/O
SR45
453Ohm
1%
/O
SC11
0.1UF/16V
/O
SR46
SR47
SR48
SR44
10KOhm
/O
/X
TACH0
SR50
0Ohm
/O
/X STP7
/X STP8
SR42
62Ohm
SR62
62Ohm
SR33
10KOhm
/O
SR35
24.9Ohm
1%
r0603_h24
SR36
SR37
SR55
SR39
SR40
SR41
SR49
SR51
SR56
10KOhm
/O
SR26
0Ohm
SR24
0Ohm
/X
SR25
0Ohm
/O
SRN5C
SRN5A
SRN5B
SRN5D
SRN4D
SRN4C
SRN4A
SRN4B
SRN9A
SRN9D
SRN9C
SRN9B
8.2KOHM
SQ19
SQ20
SQ18
SQ21
SQ17
SQ12
SQ22
SQ13
SQ16
SQ11
2N7002
PMBS3904
+VTTCPU
+5VSB
+3V
+3.3V_CL
GND
+VTTCPU_OV1#
+1.5V_OV#1
+VCORE_OV#1
S_+1.25V_OV1_Q#
S_+1.25V_OV2_Q#
O_+VTTCPU_OV#1 {65}
O_+1.5V_OV#1 {63}
O_+1.25V_OV#1 {66}
O_+1.25V_OV#2 {66}
O_+VCORE_OV#1 {60}
H_FERR#
H_THERMTRIP#
H_STPCLK#
H_SMI#
H_THERMTRIP#
H_STPCLK# R
S_TP_INIT3_3V#
S_SATARBIAS
S_SATAGP1
S_+1.25V_OV1_Q#
S_+1.25V_OV2_Q#
S_SATAGP4
S_SATAGP5
S_ICH_CL_REF
S_ICH_GPIO1
S_ICH_GPIO6
S_ICH_GPIO7
S_ICH_PWM1
S_ICH_PWM2
SIO_PECI {51}
H_PECI_SB
H_PECI_SIO {51}
T_SATALED# {59}
O_BIOS_WP# {50}
J_NOS_GATE {67}
J_CPUTM# {67}
SB_SEN_CPUFAN {57}
SB_CPUFAN_PWM {57}
O_SST {51}
CK_SB_SATA# {7}
CK_SB_SATA {7}
For the CONROE processor (BI-direction)
3個電阻需放靠近在一起以避免殘線
<Variant Name>
Title : ICH9-3
ASUSTek Computer Inc.
Engineer: Tyler_Yuan
Size A3
Project Name P5E-VM DO
Rev 1.01G
Date: Friday, March 28, 2008
Sheet 33 of 70

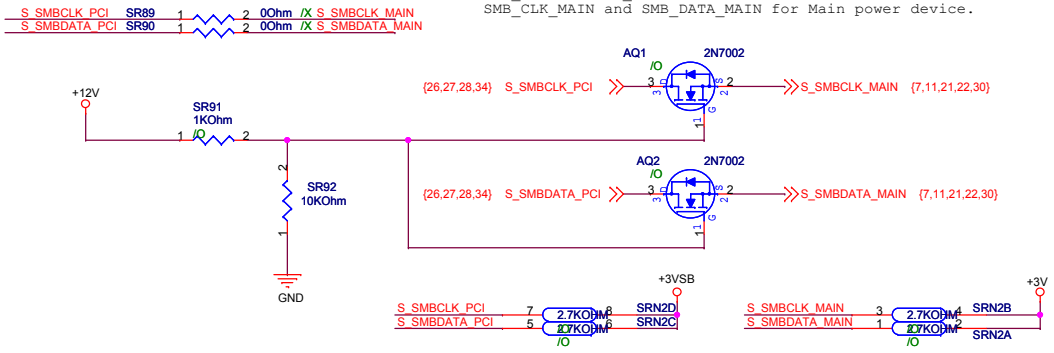

NEW CPU
+BAT_3V
SR3 1MOhm /NEWCPU
SR8 1MOhm /NEWCPU
NEW_CPU
SQ1 2N7002 /NEWCPU
{10} H_SKTOCC#
OC9 0.1UF/16V /NEWCPU
GND
RING#
SR16 8.2KOhm
SQ6
{54} O_RI1#
PMBS3904
Straping Pin:
1: X4
0: X1
SR99 15KOhm /X
SR100 15KOhm /X
{41} A_Z_SDOUT
{41} A_Z_SYNC
SR80 15KOhm /O
SR220 15KOhm /O
REMOVE FOR TCO MODE
S_SMBCLK_PCI
SR73 0Ohm /X
SMLINK0
S_SMBDATA_PCI
SR74 0Ohm /X
SMLINK1
Regin 自行更換
O_BTN1
SC6 100PF/50V /X
CL CONTROL CIRCUIT
SR79 150Ohm /AMT
S_SLP_M
{7,17,62,65}
SR84 10KOhm /AMT
S_ICH9_SLP_M#
SQ2
PMBS3904 /AMT
SC13 1UF/16V/0603 /X/AMT
SR54 10KOhm /X
{51} LDRQ0#
SR53 10KOhm /X
S_LDRQ1#
{30,49,51} F_LAD0
{30,49,51} F_LAD1
{30,49,51} F_LAD2
{30,49,51} F_LAD3
{30,49,51} F_FRAME#
SU1D
LDRQ1#/GPIO23
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
LDRQ0#
FWH4/LFRAME#
LPC
{41} A_Z_SDIN0
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
{41} A_Z_SDOUT
HDA_SDOUT
{41} A_Z_SYNC
HDA_SYNC
{8} CK_14M_SB
CLK14
{41,69} A_Z_BITCLK
HDA_BIT_CLK
{41} A_Z_RST#
HDA_RST#
AUDIO
SRN1B O_BTN1
SRN1A SMLINKALERT#
SRN1C SMLINK0
SRN1D SMLINK1
{59} O_BTN1
{26,27,28,36} S_SMBCLK_PCI
{26,27,28,36} S_SMBDATA_PCI
SMBALERT#/GPIO11
SMBCLK
SMBDATA
SMLINKALERT#
SMLINK0
SMLINK1
LINKALERT#/GPIO60/CLGPIO4
SMBUS
{51,65} S_SLPS3#
{7,64} S_SLPS4#
S_SLPS3#
S_SLPS4#
SLP_S3#
SLP_S4#
SLP_S5#
MISC
SR75 8.2K
S_ICH9_SLP_M#
{7} S_CK_PWROK
T23
T24
SLP_M#
CK_PWROK
TP0
TP1
TP2
TP3
ICH_TP0
ICH_TP1
ICH_TP2
ICH9
GPIO0
GPIO8
GPIO18
GPIO20
GPIO24
GPIO25
GPIO26
GPIO27
GPIO28
GPIO32
GPIO33
GPIO49
J_SILENT# {67}
A_FP_PRES# {42}
S_WOL_ONLY {62}
O_PME# {51}
O_PWRBTN# {51}
S_PCI_STOP# {7}
S_CPU_STOP# {7}
S_S4_STATE# {51}
PLED
MFG_MODE_N
S_GPIO49
SR60 2.2KOhm
R1.01G
DMI TERMINATION STRAP
SR67 390KOhm
SR65 8.2K
TO ENABLE INTERNAL VRM
SR52 8.2K
{42} A_FP_PRES#
INTRUDER#
LAN100_SLP
THRM#
MCH_SYNC#
SUS_STAT#/LPCPD
SUSCLK
GPIO34
GPIO56
CLGPIO5/GPIO57
NEW_CPU
EnableLANPower
ICH_THERM#
N_ICH9_SYNC# {17}
S_PWRDWN# {30,49}
S_SUSCLK
S_GPIO56
SR70 10KOhm
SR57 10KOhm
T22
SR71 1KOhm
SR72 8.2K
Regin 預留 ,Cost Down
SR6 8.2K
ICH_VRMPGD
WAKE#
PWRBTN#
RI#
CPUPWRGD
VRMPWRGD
PWROK
X_WAKE# {26,27}
O_PWRBTN# {51}
RING#
H_CPUPWRGD {10,11}
P_VRM_GD {60,62}
O_PWROK {7,17,51}
PLTRST#
SYS_RESET#
RSMRST#
S_PLTRST# {17,30,40,49,51}
O_RSTCON# {7,11,59}
O_RSMRST# {7,29,51}
TO ENABLE INTERNAL VRM
SR77 390KOhm
INTVRMEN
Trap for TCO timer reboot feature
SR76 1KOhm /X
SR78 4.7KOhm
SPKR
S_SPKR {59}
SR69 4.7KOhm
SERVICE_MODE
MFG_MODE_N
HEADER_1X3P
Power LED
S_PLED- {59}
PLED
R3 8.2KOhm
SQ3
PMBS3904
<Variant Name>
Title : ICH9-4
ASUSTek Computer Inc.
Engineer: Tyler_Yuan
Size A3
Project Name P5E-VM DO
Rev 1.01G
Date: Friday, March 28, 2008
Sheet 34 of 70

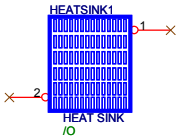

1.05V LAN OUTPUT
P_+1P05V_LAN
SC14 1UF/10V c0603 /O
SC15 0.1UF/16V /O
SU1E
ICH9 /O
+1.5V
SC18 1UF/10V
SC19 1UF/10V
SC20 0.1UF/16V
SC21 0.1UF/16V
+VTTCPU
SC89 0.1UF/16V /O
SC26 0.1UF/16V /X
SC90 4.7UF/6.3V /X
V5REF_SUS
V5REF
SR81 10Ohm
SR82 10Ohm
+5VSB
+5V
+3V
SD2 BAT54CW /O
SC16 0.1UF/16V /O
SC17 0.1UF/16V /O
P_+1.5V_PCIE
L1 1UH
SC22 22UF/6.3V /O c0805
SC23 22UF/6.3V /O c0805
SC24 2.2UF/6.3V /O c0603
SC25 4.7UF/6.3V
SCE1 330uF/6.3V
+3V
SC27 0.1UF/16V /O
SC28 0.1UF/16V /O
SC29 0.1UF/16V /X
SC30 0.1UF/16V /X
SC31 0.1UF/16V /X
SC32 0.1UF/16V /O
SC33 0.1UF/16V /O
SC34 0.1UF/16V /X
+3.3V_CL
SC41 0.1UF/16V /O
+3VSB
SC42 0.1UF/16V /O
SC43 0.1UF/16V /O
SC48 1UF/10V
SC49 1UF/10V
SC50 0.1UF/16V /X
SC51 0.1UF/16V /X
SC52 0.1UF/16V /O
+BAT_3V
SC55 1UF/10V c0603 /X
SC56 0.1UF/16V /X
SC57 0.1UF/16V /O
P_+1.05VSB_INT_A
P_+1.05VSB_INT_B
P_+1.5VSB_INT
SC58 1UF/10V
SC59 0.1UF/16V /O
SC2 0.1UF/16V /O
R1.01G
+1.25V
+1P25V_VCCDMI
SR83 0Ohm
SC37 1UF/10V
SC38 22UF/6.3V /O c0805
+1.05V
SC44 0.022UF/16V /O
SC47 0.1UF/16V /X
+1.5V
VCCSATA_PLL
SL1 10UH
SC35 1UF/10V c0603 /O
SC36 10UF/6.3V /O
+1P5V_GLAN_PLL
SL2 1UH
SC39 1UF/10V
SC40 10UF/6.3V /X
+1P5V_DMIPLL
SL3 1UH
SC53 0.01UF/50V /O
SC54 10UF/6.3V /O
P_+1.5VCL_INT
P_+1.05VSB_CL_INT
SC62 1UF/10V
SC63 0.1UF/16V /X
SC60 0.1UF/16V /O
SC61 1UF/10V c0603 /O
SC64 0.1UF/16V /O
GND
<Variant Name>
Title : ICH9-5
ASUSTek Computer Inc.
Engineer: Tyler_Yuan
Size A3
Project Name P5E-VM DO
Rev 1.01G
Date: Friday, March 28, 2008
Sheet 35 of 70



SMBus Switch

1.00 SMBus connect to two kind of devices, one use Main power, another use Standby power, so use this switch circuit to isolate those two device.
SMB_CLK and SMB_DATA for Standby device.
SMB_CLK_MAIN and SMB_DATA_MAIN for Main power device.





<Variant Name>

ASUSTek Computer Inc.	Title : ICH9-6	
	Engineer: Tyler_Yuan	
Size: A3	Project Name: P5E-VM DO	Rev: 1.01G
Date: Friday, March 28, 2008	Sheet 36 of 70	

0.2A Beta

If the PCI chipset can support 3.3v and 5v signaling, then connect the PCI_VIOS pin on the FW322 to the PCI_VIO pin (A59)

ZR1 for crystal oscillator stability

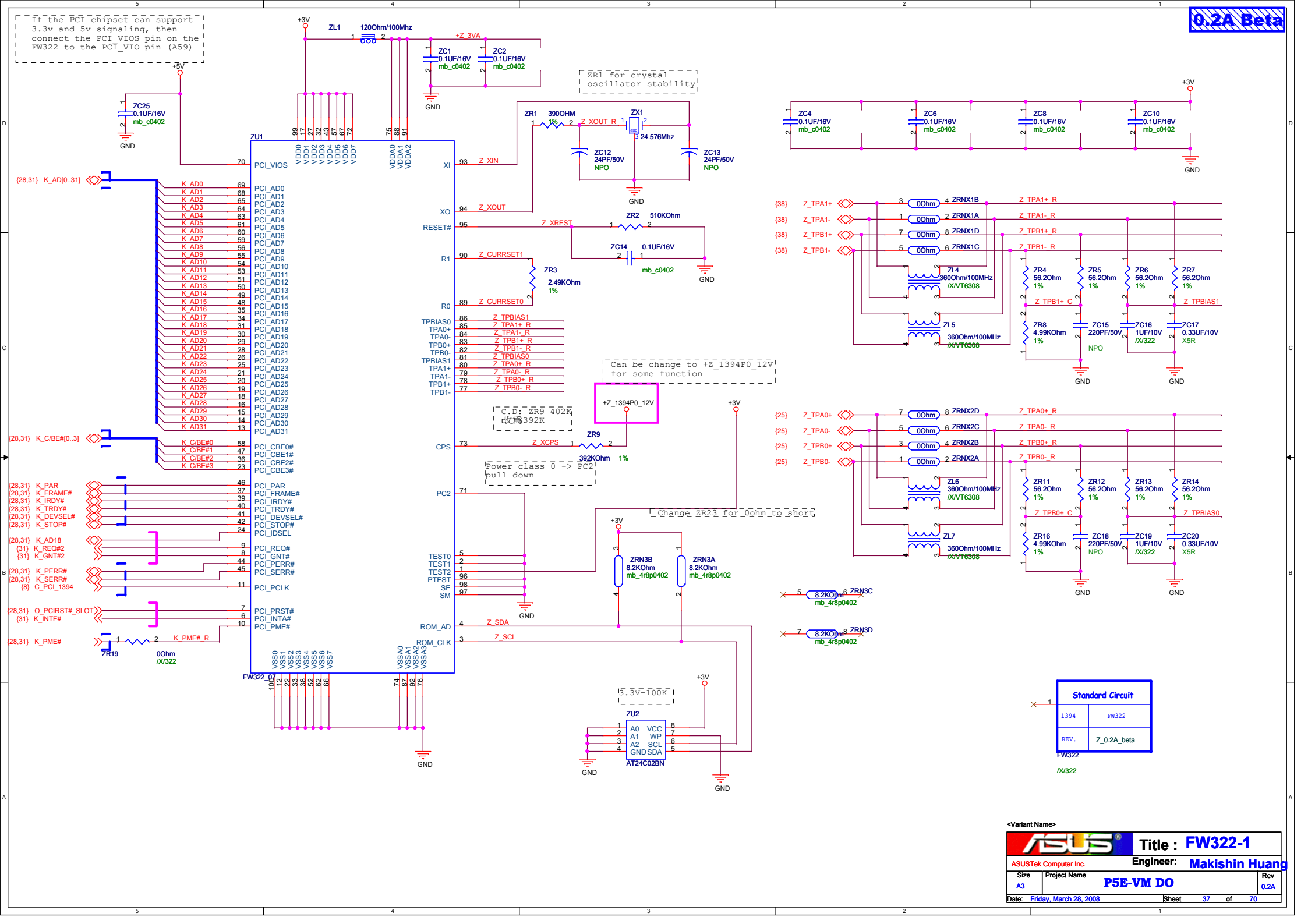
Can be change to +Z_1394P0_12V for some function

C.D: ZR9 402K 改為392K

Power class 0 -> PC2 pull down

Change ZR23 for 0ohm to short

3.3V-100K



<Variant Name>

ASUSTek Computer Inc.

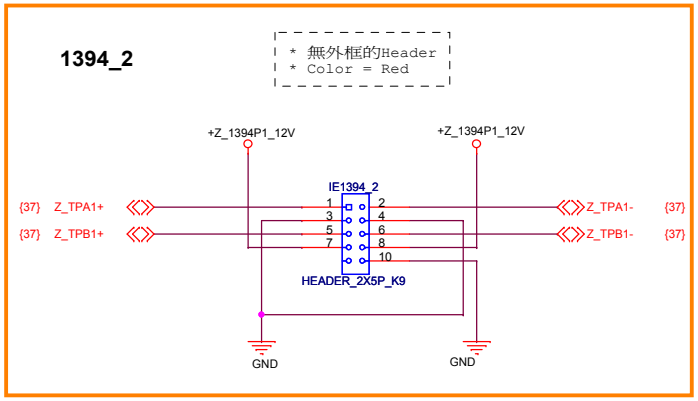
Title : FW322-1

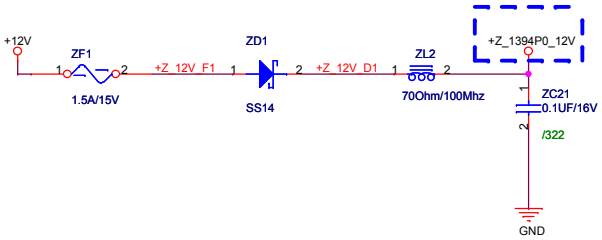
Engineer: Makishin Huang

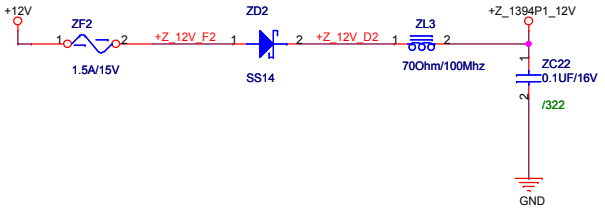
Size	Project Name	Rev
A3	P5E-VM DO	0.2A

Date: Friday, March 28, 2008 Sheet 37 of 70

0.2A Beta







<Variant Name>

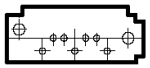
ASUSTek Computer Inc.

Title : FW322-2

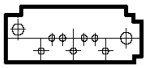
Engineer: Makishin Huang

Size	Project Name	Rev
A3	P5E-VM DO	0.2A

Date: Friday, March 28, 2008 Sheet 38 of 70



顏色：Black

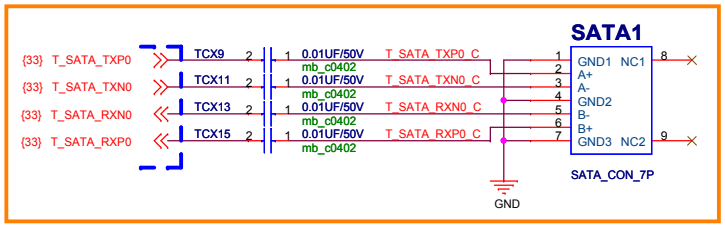


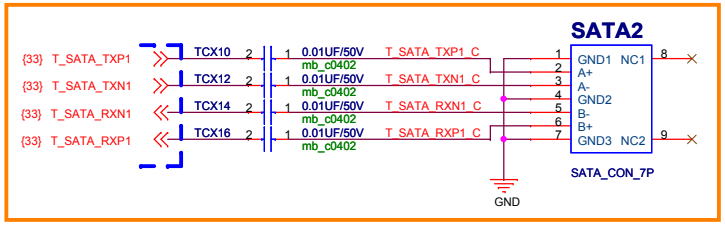
顏色：RED

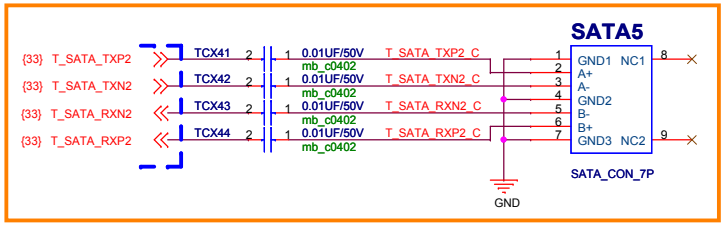
0.2A Beta

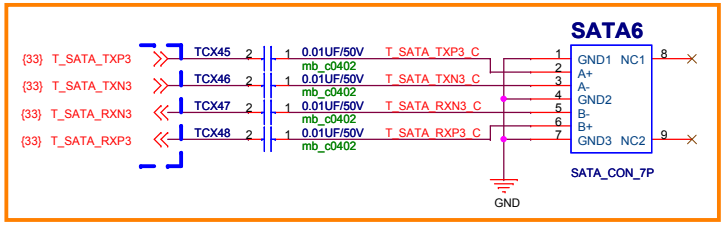
（1）假如Chipset沒有分Master & Slave, Connector顏色請選擇黑色.

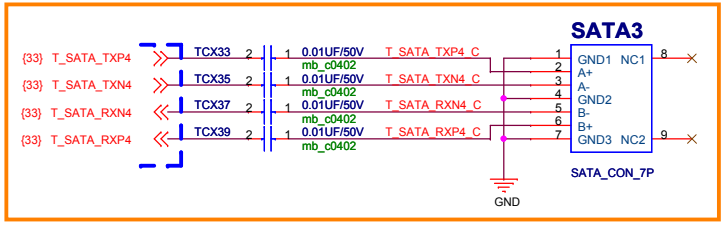
（2）假如Chipset有分Master & Slave, Masterr顏色請選擇紅色Connector Slave顏色請選擇黑色Connector

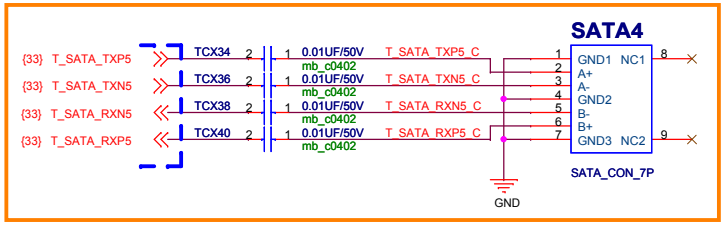


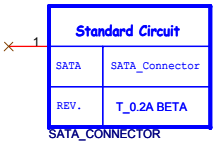












<Variant Name>

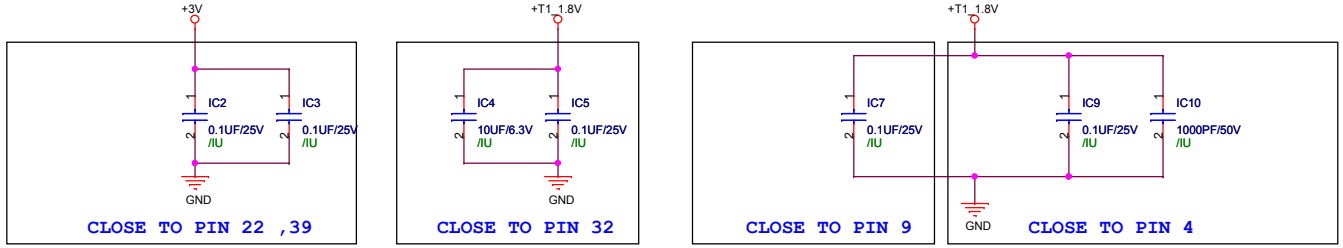
ASUSTek Computer Inc.

Title : SATA_Connector

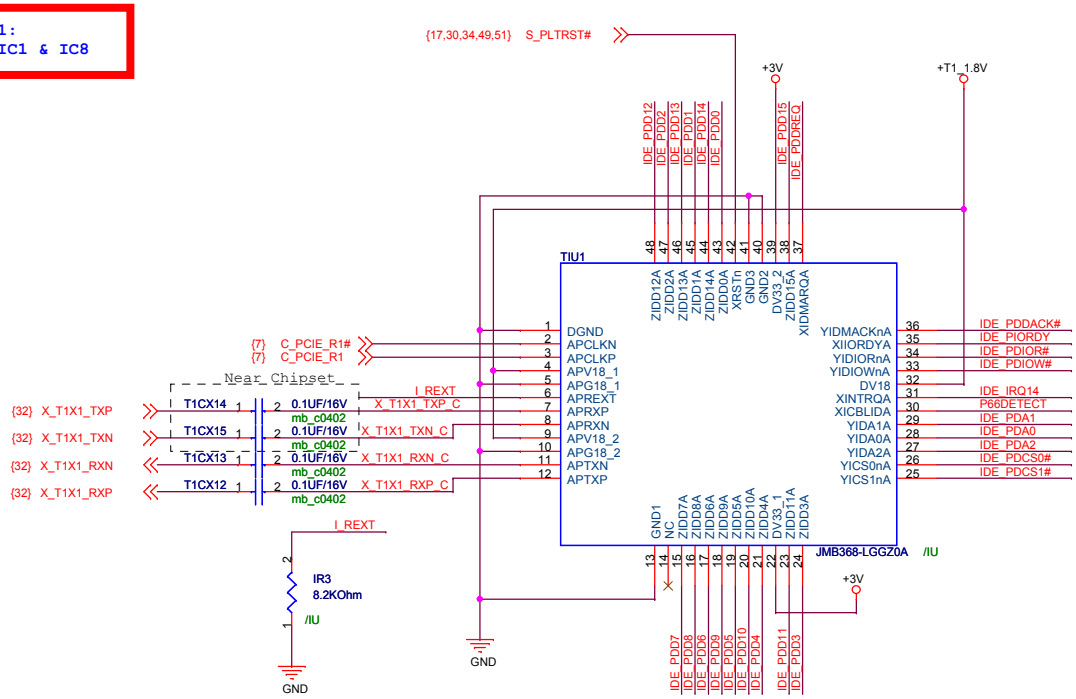
Engineer: David Yao

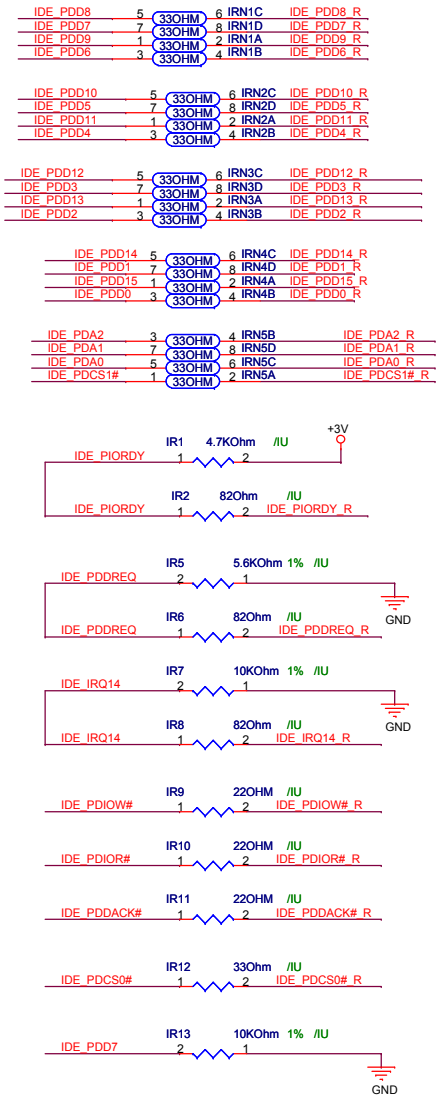
Size	Project Name	Rev
A3	P5E-VM DO	0.2A

Date: Friday, March 28, 2008 Sheet 39 of 70

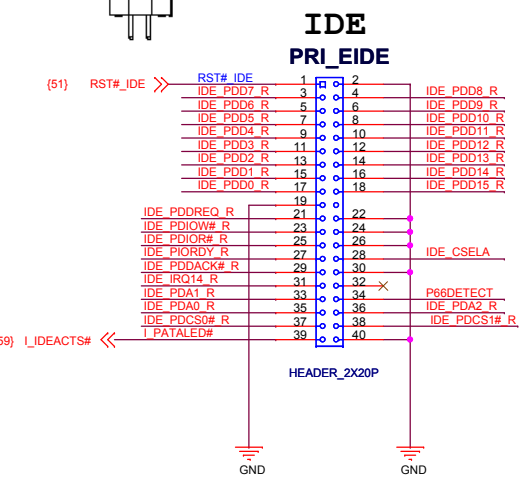


R1.01:
拿掉IC1 & IC8

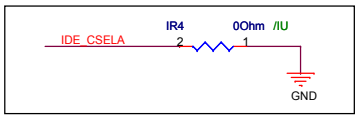




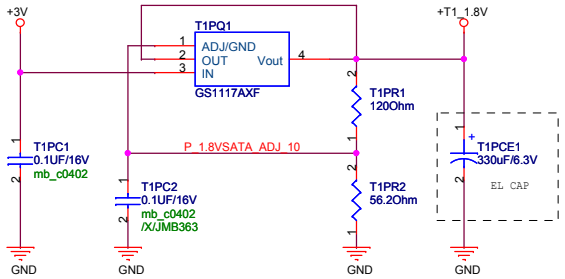
PRI_IDE (垂直) Color : RED



ST connector PN:12G07120040K (Blue)
R/A connector PN:12G07110040K (Blue)
R/A connector PN:12G07110040N (Red)



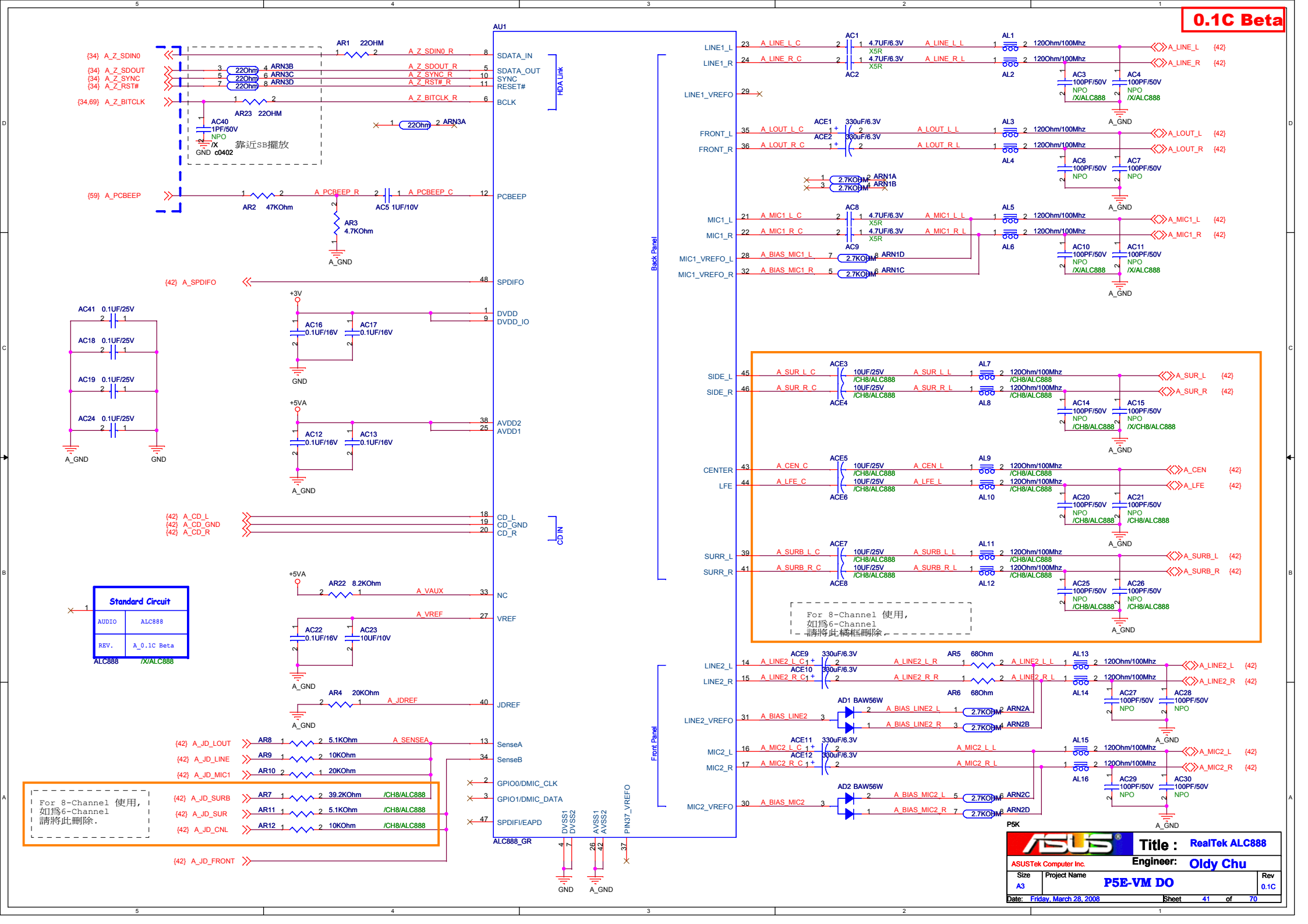
+T1_1.8V
Io=0.5A



Vout=Vref(1+T1PR2/T1PR1)=1.25*(1+56.2/120)=1.835V*

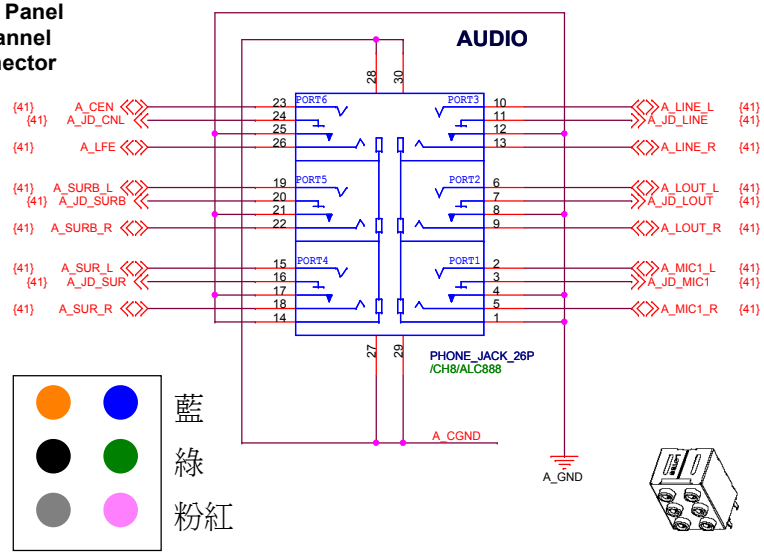
<Variant Name>

ASUSTeK COMPUTER INC	Title : <Title>	
	Engineer: Regin_Chiang	
Size: A3	Project Name: P5E-VM DO	Rev: 1.00
Date: Friday, March 28, 2008	Sheet 40 of 70	

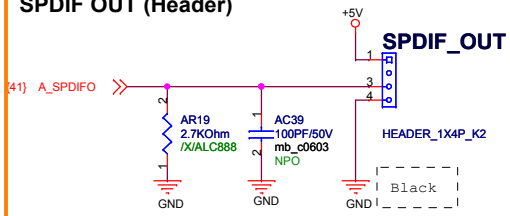

0.1C Beta
AU1
SDATA_IN
SDATA_OUT
SYNC
RESET#
BCLK
HDA Link
PCBEEP
SPDIFO
DVDD
DVDD_IO
AVDD2
AVDD1
CD_L
CD_GND
CD_R
CD IN
NC
VREF
JDREF
SenseA
SenseB
GPIO0/DMIC_CLK
GPIO1/DMIC_DATA
SPDIFI/EAPD
DVSS1
DVSS2
AVSS1
AVSS2
PIN37_VREFO
ALC888_GR
Back Panel
Front Panel
LINE1_L
LINE1_R
LINE1_VREFO
FRONT_L
FRONT_R
MIC1_L
MIC1_R
MIC1_VREFO_L
MIC1_VREFO_R
SIDE_L
SIDE_R
CENTER
LFE
SURR_L
SURR_R
LINE2_L
LINE2_R
LINE2_VREFO
MIC2_L
MIC2_R
MIC2_VREFO
A_Z_SDIN0
A_Z_SDOUT
A_Z_SYNC
A_Z_RST#
A_Z_BITCLK
A_PCBEEP
A_SPDIFO
A_CD_L
A_CD_GND
A_CD_R
A_VAUX
A_VREF
A_JDREF
A_SENSEA
A_JD_LOUT
A_JD_LINE
A_JD_MIC1
A_JD_SURB
A_JD_SUR
A_JD_CNL
A_JD_FRONT
A_GND
GND
+3V
+5VA
P5K
Standard Circuit
AUDIO
ALC888
REV.
A_0.1C Beta
ALC888
/X/ALC888
For 8-Channel 使用,
如爲6-Channel
請將此橘框刪除.
For 8-Channel 使用,
如爲6-Channel
請將此刪除.
靠近SB擺放
ASUSTek Computer Inc.
Title : RealTek ALC888
Engineer: Oldy Chu
Size A3
Project Name P5E-VM DO
Rev 0.1C
Date: Friday, March 28, 2008
Sheet 41 of 70

0.1C Beta

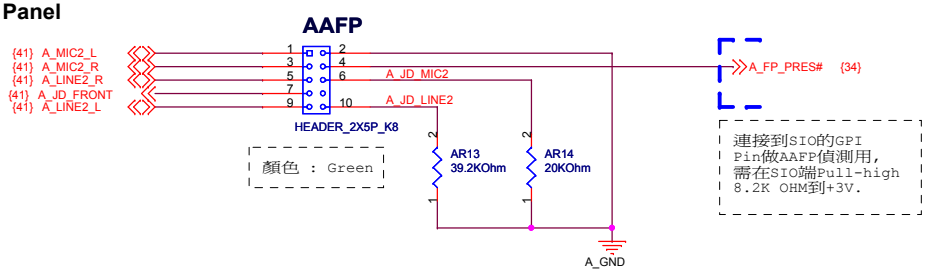
Back Panel 8 Channel Connector



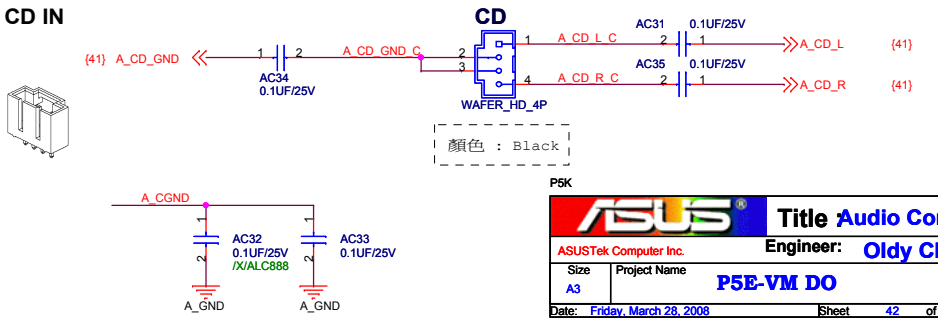
SPDIF OUT (Header)



Front Panel

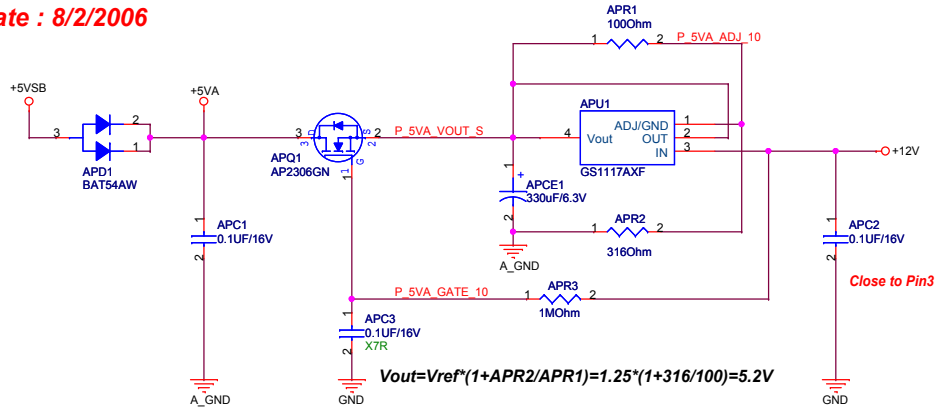


CD IN



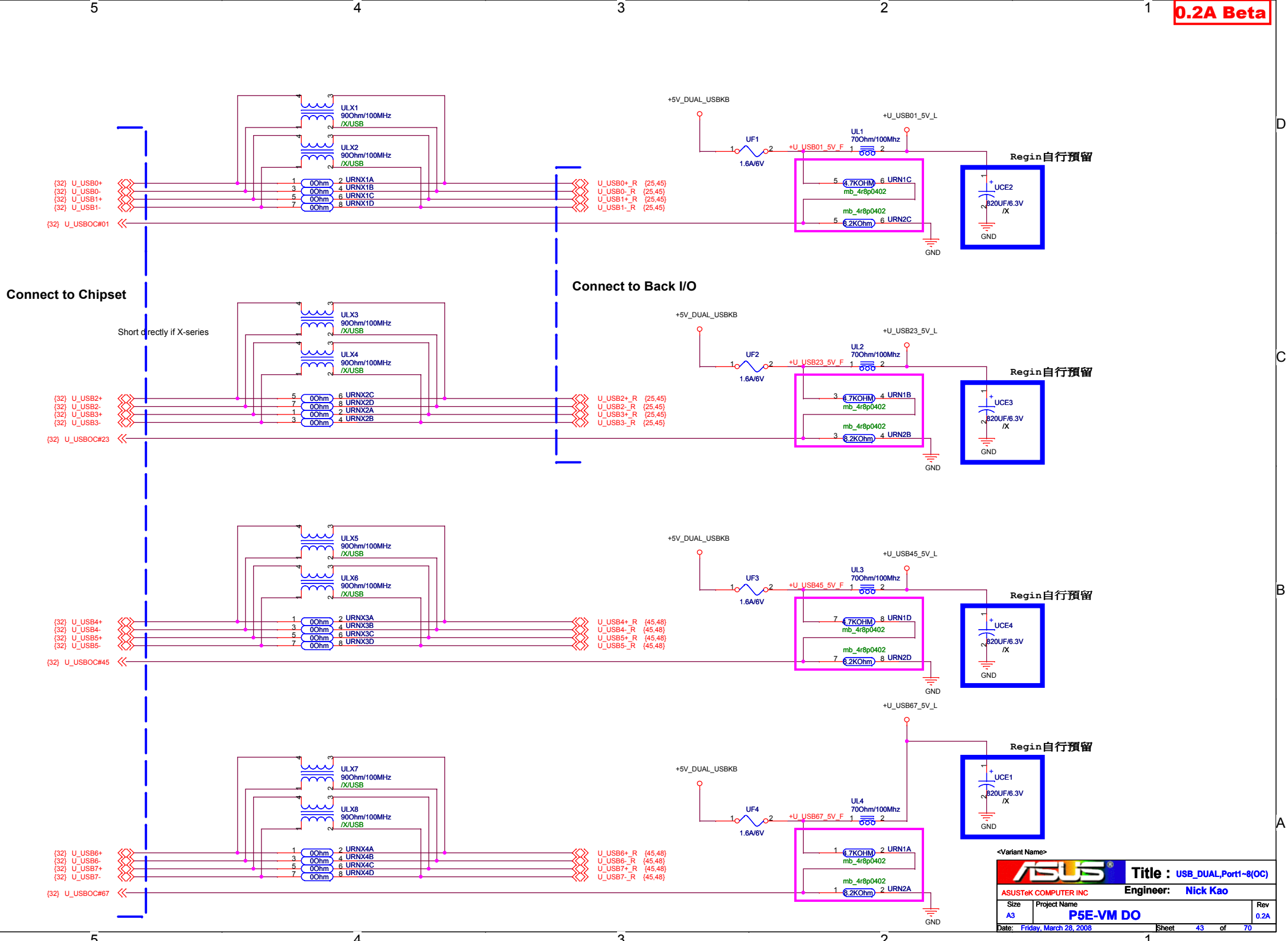
Audio Codec New Solution for Vista !!

Date : 8/2/2006

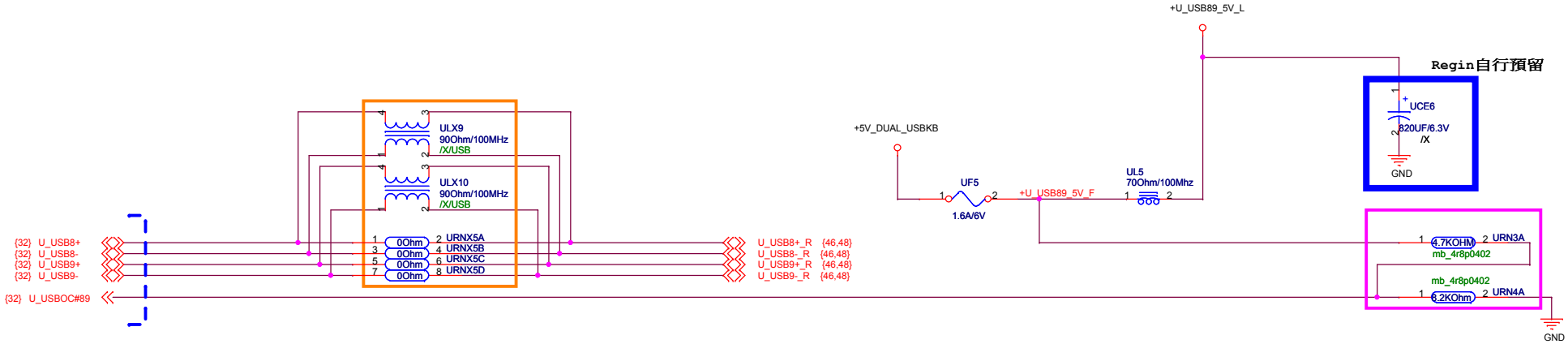


P5K

ASUSTek Computer Inc.	Title: Audio Connector	
	Engineer: Oldy Chu	
Size: A3	Project Name: P5E-VM DO	Rev: 0.1C
Date: Friday, March 28, 2008	Sheet 42 of 70	

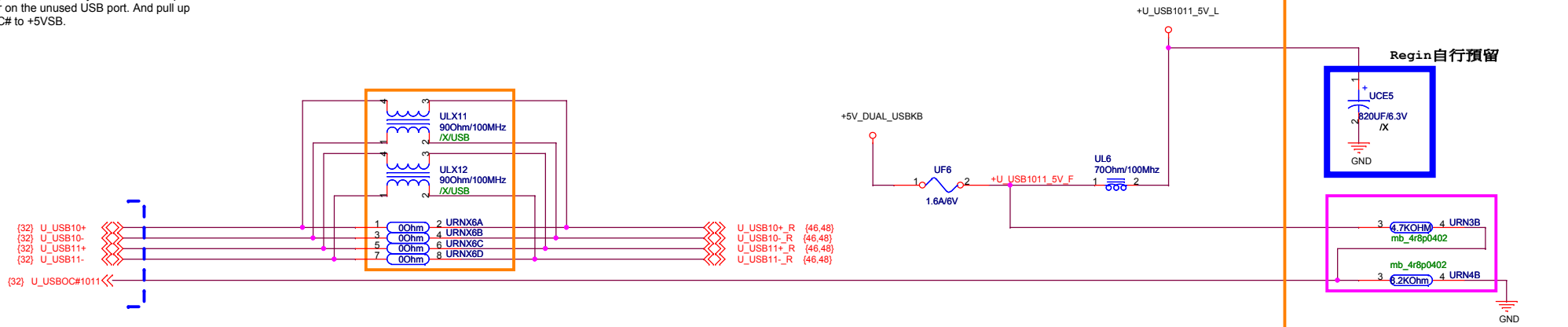

0.2A Beta
Connect to Chipset
Connect to Back I/O
Short directly if X-series
ULX1
90Ohm/100MHz
/X/USB
ULX2
90Ohm/100MHz
/X/USB
ULX3
90Ohm/100MHz
/X/USB
ULX4
90Ohm/100MHz
/X/USB
ULX5
90Ohm/100MHz
/X/USB
ULX6
90Ohm/100MHz
/X/USB
ULX7
90Ohm/100MHz
/X/USB
ULX8
90Ohm/100MHz
/X/USB
{32} U_USB0+
{32} U_USB0-
{32} U_USB1+
{32} U_USB1-
{32} U_USBOC#01
{32} U_USB2+
{32} U_USB2-
{32} U_USB3+
{32} U_USB3-
{32} U_USBOC#23
{32} U_USB4+
{32} U_USB4-
{32} U_USB5+
{32} U_USB5-
{32} U_USBOC#45
{32} U_USB6+
{32} U_USB6-
{32} U_USB7+
{32} U_USB7-
{32} U_USBOC#67
0Ohm
URNX1A
URNX1B
URNX1C
URNX1D
URNX2C
URNX2D
URNX2A
URNX2B
URNX3A
URNX3B
URNX3C
URNX3D
URNX4A
URNX4B
URNX4C
URNX4D
U_USB0+_R {25,45}
U_USB0-_R {25,45}
U_USB1+_R {25,45}
U_USB1-_R {25,45}
U_USB2+_R {25,45}
U_USB2-_R {25,45}
U_USB3+_R {25,45}
U_USB3-_R {25,45}
U_USB4+_R {45,48}
U_USB4-_R {45,48}
U_USB5+_R {45,48}
U_USB5-_R {45,48}
U_USB6+_R {45,48}
U_USB6-_R {45,48}
U_USB7+_R {45,48}
U_USB7-_R {45,48}
+5V_DUAL_USBKB
UF1
UF2
UF3
UF4
1.6A/6V
+U_USB01_5V_L
+U_USB23_5V_L
+U_USB45_5V_L
+U_USB67_5V_L
+U_USB01_5V_F
+U_USB23_5V_F
+U_USB45_5V_F
+U_USB67_5V_F
UL1
UL2
UL3
UL4
70Ohm/100Mhz
4.7KOHM
6.2KOhm
mb_4r8p0402
URN1C
URN2C
URN1B
URN2B
URN1D
URN2D
URN1A
URN2A
GND
Regin自行預留
UCE1
UCE2
UCE3
UCE4
820UF/6.3V
/X
<Variant Name>
Title : USB_DUAL,Port1~8(OC)
ASUSTeK COMPUTER INC
Engineer: Nick Kao
Size A3
Project Name P5E-VM DO
Rev 0.2A
Date: Friday, March 28, 2008
Sheet 43 of 70

If there are unused USB ports,you need check with the chipset vendor.It may need to have a pull down resistor on the unused USB port. And pull up USBOC# to +5VSB.



C.2

If there are unused USB ports,you need check with the chipset vendor.It may need to have a pull down resistor on the unused USB port. And pull up USBOC# to +5VSB.



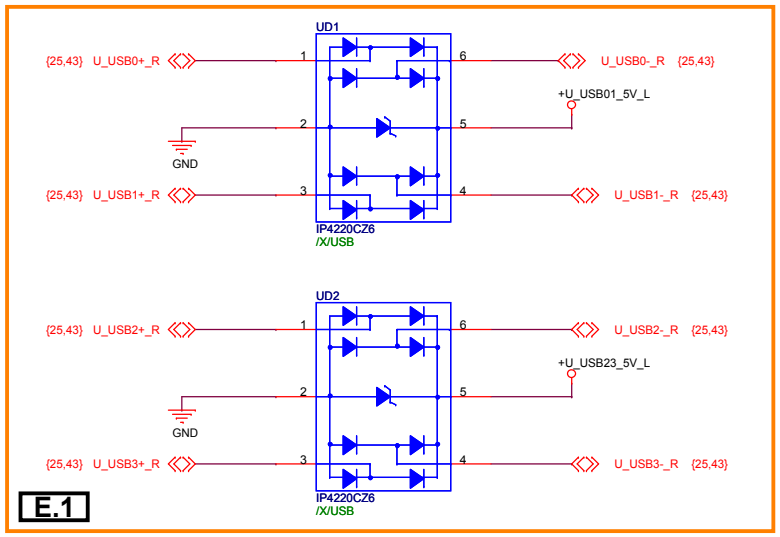
<Variant Name>

ASUSTeK COMPUTER INC	Title : USB_DUAL,Port9~12(OC)	
	Engineer: Nick Kao	
Size: A3	Project Name: P5E-VM DO	Rev: 0.2A
Date: Friday, March 28, 2008	Sheet 44 of 70	

0.2A Beta

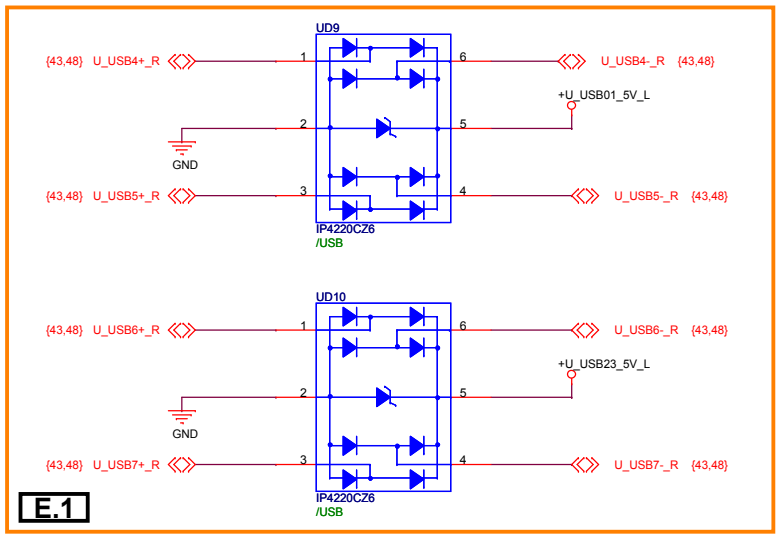
Back I/O USB ESD Protection (IP4220CZ6 or BAV99)
Port 1~4

一般使用BAV99，使用IP4220CZ6需主管Review同意



Back I/O USB ESD Protection (IP4220CZ6 or BAV99)
Port 5~8

一般使用BAV99，使用IP4220CZ6需主管Review同意



<Variant Name>

Title :USB_DUAL,Port 1~8 (ESD)

ASUSTeK COMPUTER INC

Engineer: Nick Kao

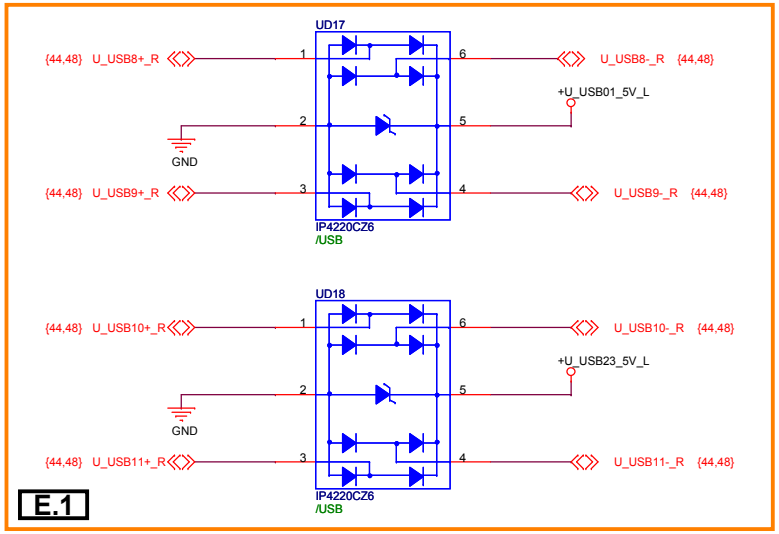
Size	Project Name	Rev
A3	P5E-VM DO	0.2A

Date: Friday, March 28, 2008 Sheet 45 of 70

0.2A Beta

Back I/O USB ESD Protection (IP4220CZ6 or BAV99)
Port 5~8

一般使用BAV99，使用IP4220CZ6需主管Review同意



<Variant Name>

ASUSTeK COMPUTER INC

Title : USB_DUAL,Port 9~12 (ESD)

Engineer: Nick Kao

Size	Project Name	Rev
A3	P5E-VM DO	0.2A

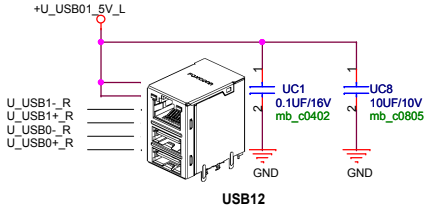
Date: Friday, March 28, 2008 Sheet 46 of 70

0.2A Beta

Connect to Back I/O

USB12

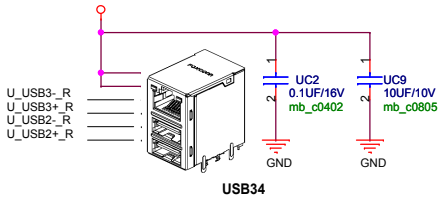
Choose a proper connector in page "Back I/O Connector"



USB12

USB34

Choose a proper connector in page "Back I/O Connector"



USB34

<Variant Name>

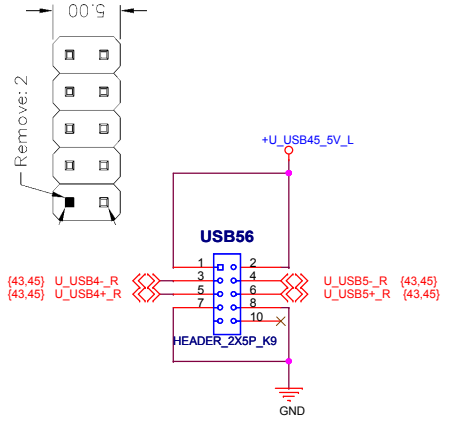
ASUSTeK COMPUTER INC	Title : USB,Port1~2(Ext.)	
	Engineer: Nick Kao	
Size: A3	Project Name: P5E-VM DO	Rev: 0.2A
Date: Friday, March 28, 2008	Sheet 47 of 70	

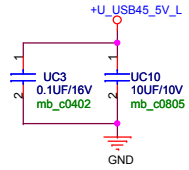
0.2A Beta

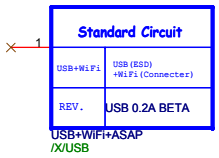
USB56 Internal Connector

Tow choice:
Box Header or Pin Header

Pin Header





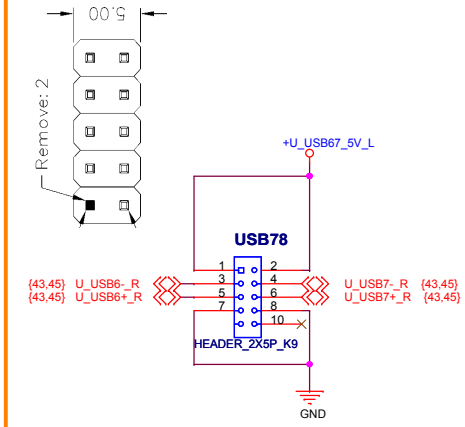


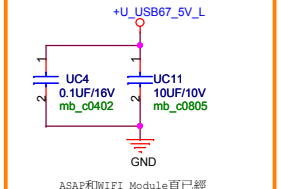
USB+WIFI+ASAP
/X/USB

USB78 Internal Connector

Tow choice:
Box Header or Pin Header

Pin Header



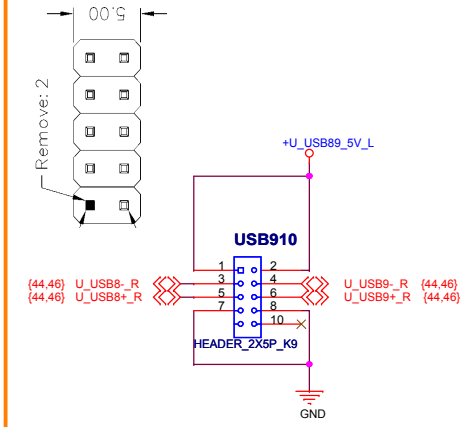


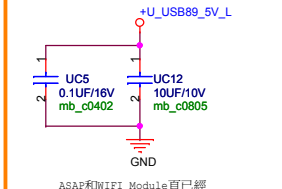
ASAP和WIFI Module頁已經
保留了電容，如果此Port不
上Box Header(Pin Header)
而上ASAP或WIFI Module
，可以連電容
一起刪掉

USB910 Internal Connector

Tow choice:
Box Header or Pin Header

Pin Header



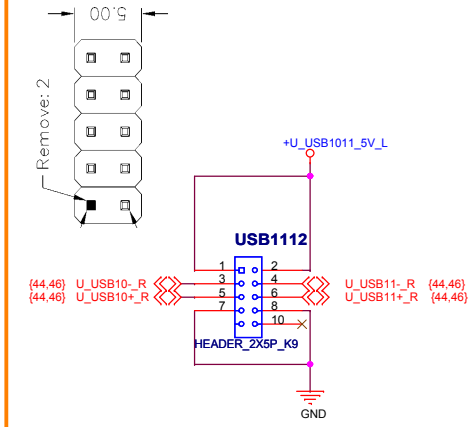


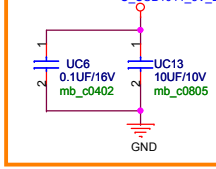
ASAP和WIFI Module頁已經
保留了電容，如果此Port不
上Box Header(Pin Header)
而上ASAP或WIFI Module
，可以連電容
一起刪掉

USB1112 Internal Connector

Tow choice:
Box Header or Pin Header

Pin Header



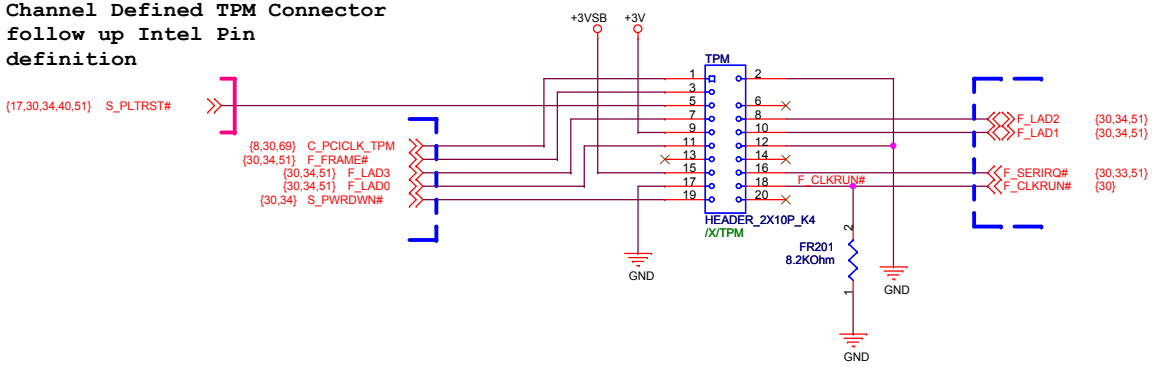


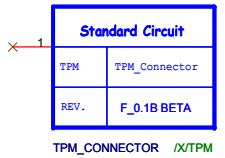
ASAP和WIFI Module頁已經
保留了電容，如果此Port不
上Box Header(Pin Header)
而上ASAP或WIFI Module
，可以連電容
一起刪掉

<Variant Name>

ASUSTeK COMPUTER INC	Title : USB,Port3~12(Int.)	
	Engineer: Nick Kao	
Size: A3	Project Name: P5E-VM DO	Rev: 0.2A
Date: Friday, March 28, 2008	Sheet 48 of 70	

Channel Defined TPM Connector follow up Intel Pin definition





<Variant Name>

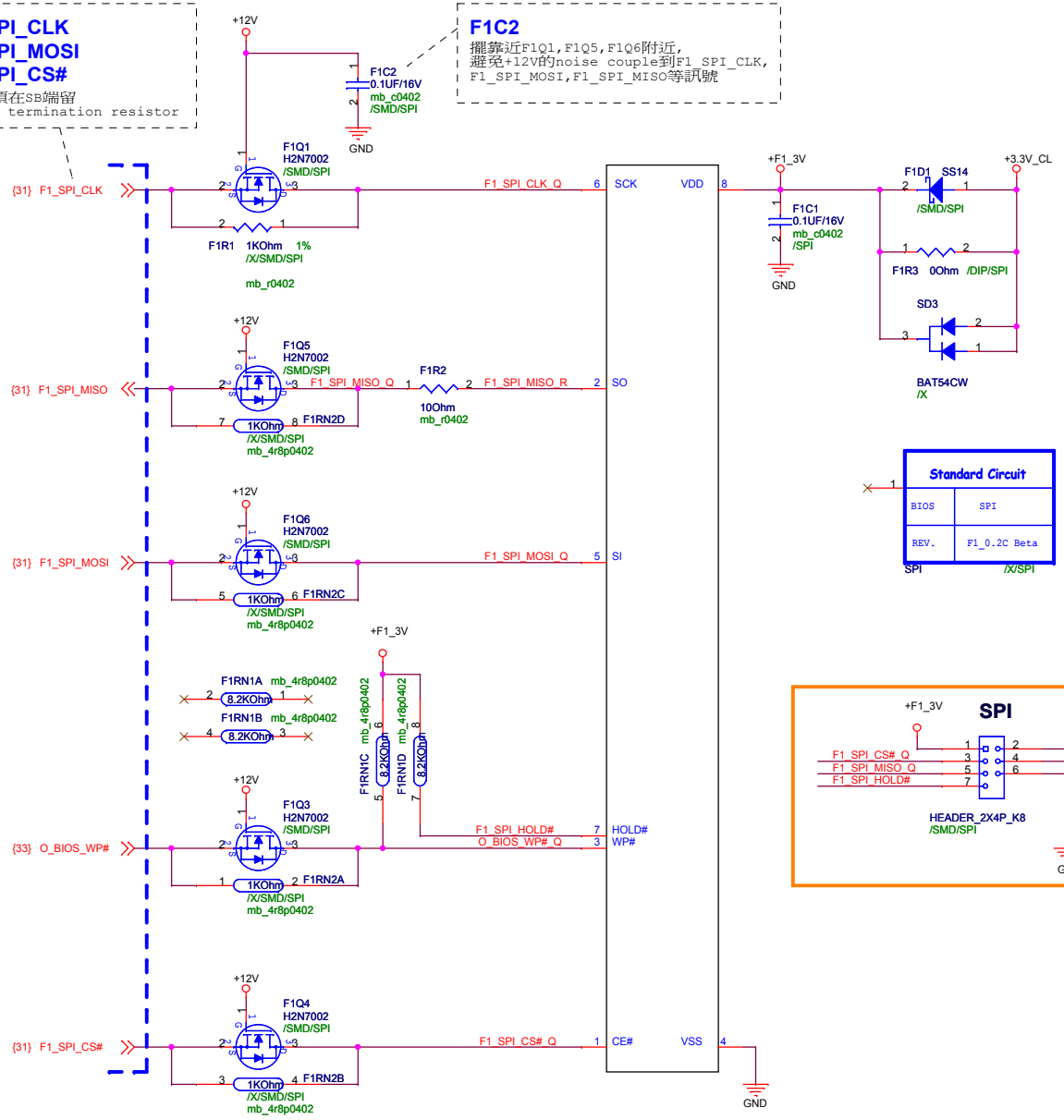
ASUSTek Computer Inc.	Title : TPM_Connector	
	Engineer: Oldy Chu	
Size: A3	Project Name: P5E-VM DO	Rev: 0.1B
Date: Friday, March 28, 2008	Sheet 49 of 70	

0.2C Beta

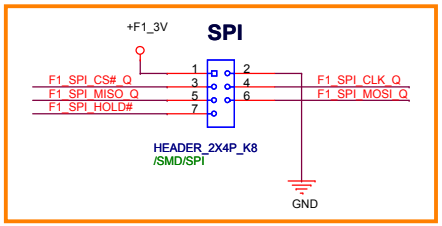
F1_SPI_CLK
F1_SPI_MOSI
F1_SPI_CS#
等net須在SB端留
series termination resistor

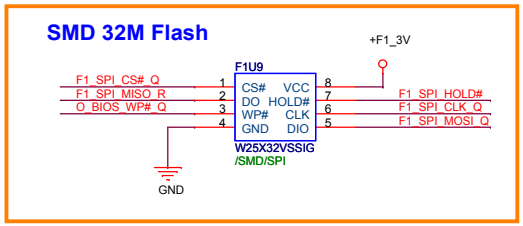
F1C2
擺靠近F1Q1,F1Q5,F1Q6附近,
避免+12V的noise couple到F1_SPI_CLK,
F1_SPI_MOSI,F1_SPI_MISO等訊號

選擇BOM要上的Flash,其餘請刪除.



Standard Circuit	
BIOS	SPI
REV.	F1_0.2C Beta
SPI	/X/SPI





SPI SMD 4M Flash P/N

Priority 1
SST : 05G00100H210

Priority 2
PMC : 05G001015311

Priority 3
ATMEL : 05G00100L010

Priority 4
Winbond : 05G00100F130

SPI SMD 8M Flash P/N

Priority 1
ST : 05G001208031
Priority 2
SST : 05G00120A010
Priority 3
MXIC : 05G001217012
Priority 4
Winbond : 05G001208130
Priority 5
ATMEL : 05G00120B010

SPI SMD 16M Flash P/N

Priority 1
SST : 05G001405010
Priority 2
MXIC : 05G001403010
Priority 3
ST : 05G001418020
Priority 4
ATMEL : 05G001409010
Priority 5
SPANSION: 05G001405111

SPI SMD 32M Flash P/N

Priority 1
Winbond : 05G00160D110

DIP & SMD SPI FLASH CO-LAYOUT BOM OPTIONAL :

DIP SPI FLASH BOM OPTIONAL :
選擇 /DIP/SPI & /X/SPI & /SPI

F1Q1,F1Q5,F1Q6,F1Q3,F1Q4,
F1C2,SPI,F1D1
BOM Optional選擇不上.

F1RN2及F1R1請RD手動改上0 ohm
F1RN2 : 10V253000040
F1R1 : 10V213000040

SMD SPI FLASH BOM OPTIONAL :
選擇/X/SMD/SPI & /SMD/SPI
/X/SPI & /SPI

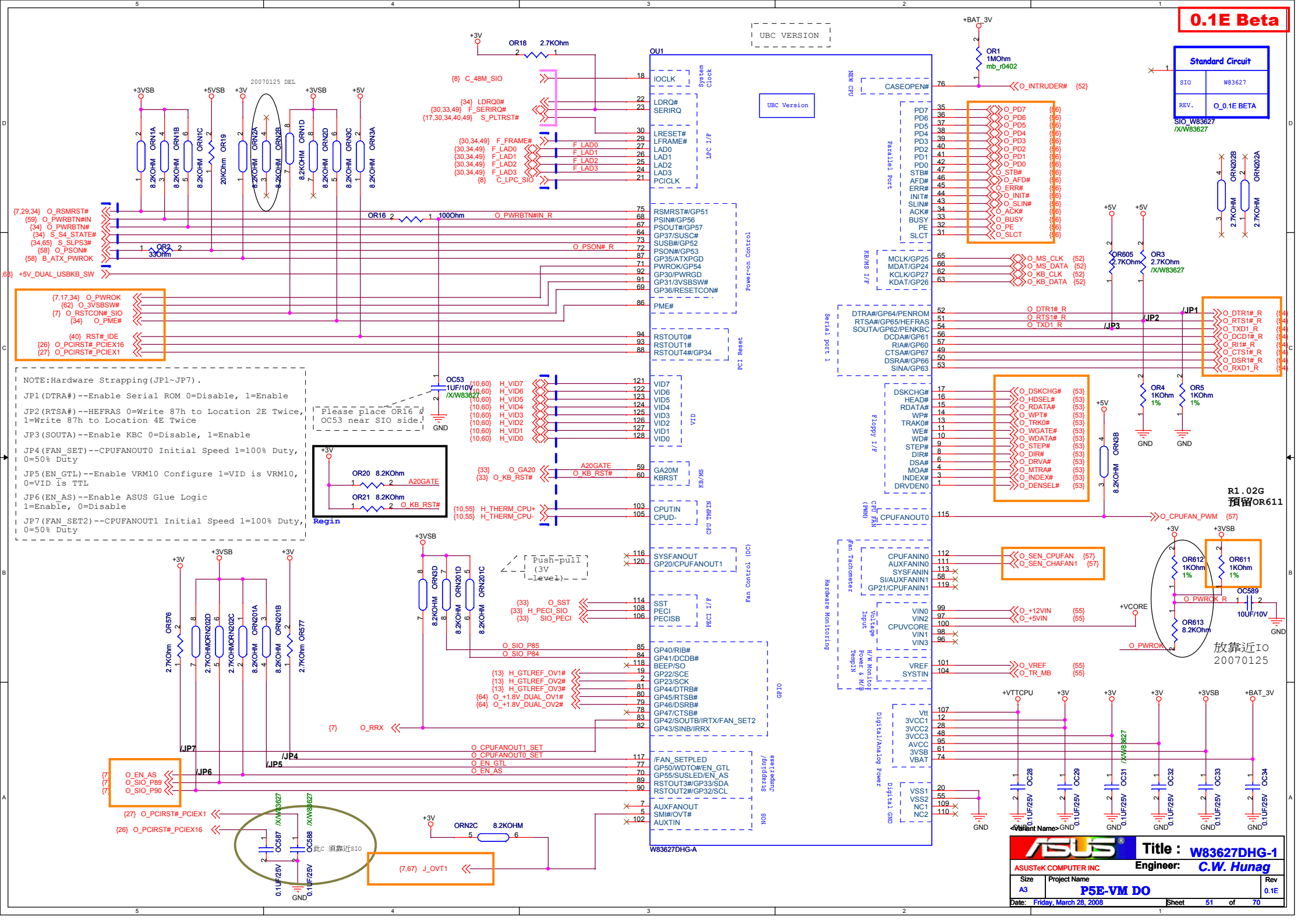
<Variant Name>

ASUSTek Computer Inc.

Title : SPI
Engineer: Eddie Chiu

Size	Project Name	Rev
A3	P5E-VM DO	0.2C

Date: Friday, March 28, 2008 Sheet 50 of 70

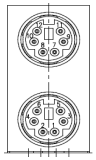

0.1E Beta
UBC VERSION
UBC Version
OU1
W83627DHG-A
NOTE:Hardware Strapping(JP1~JP7).
JP1(DTRA#)--Enable Serial ROM 0=Disable, 1=Enable
JP2(RTSA#)--HEFRAS 0=Write 87h to Location 2E Twice, 1=Write 87h to Location 4E Twice
JP3(SOUTA)--Enable KBC 0=Disable, 1=Enable
JP4(FAN_SET)--CPUFANOUT0 Initial Speed 1=100% Duty, 0=50% Duty
JP5(EN_GTL)--Enable VRM10 Configure 1=VID is VRM10, 0=VID is TTL
JP6(EN_AS)--Enable ASUS Glue Logic 1=Enable, 0=Disable
JP7(FAN_SET2)--CPUFANOUT1 Initial Speed 1=100% Duty, 0=50% Duty
Please place OR16 & OC53 near SIO side.
Regin
Push-pull (3V level)
Standard Circuit
SIO W83627
REV. O_0.1E BETA
SIO_W83627
/X/W83627
R1.02G
預留OR611
放靠近IO
20070125
Title : W83627DHG-1
ASUSTeK COMPUTER INC
Engineer: C.W. Hunag
Size A3
Project Name P5E-VM DO
Rev 0.1E
Date: Friday, March 28, 2008
Sheet 51 of 70

0.1C Beta

1.Please choose KB_USB56 or KBMS connector

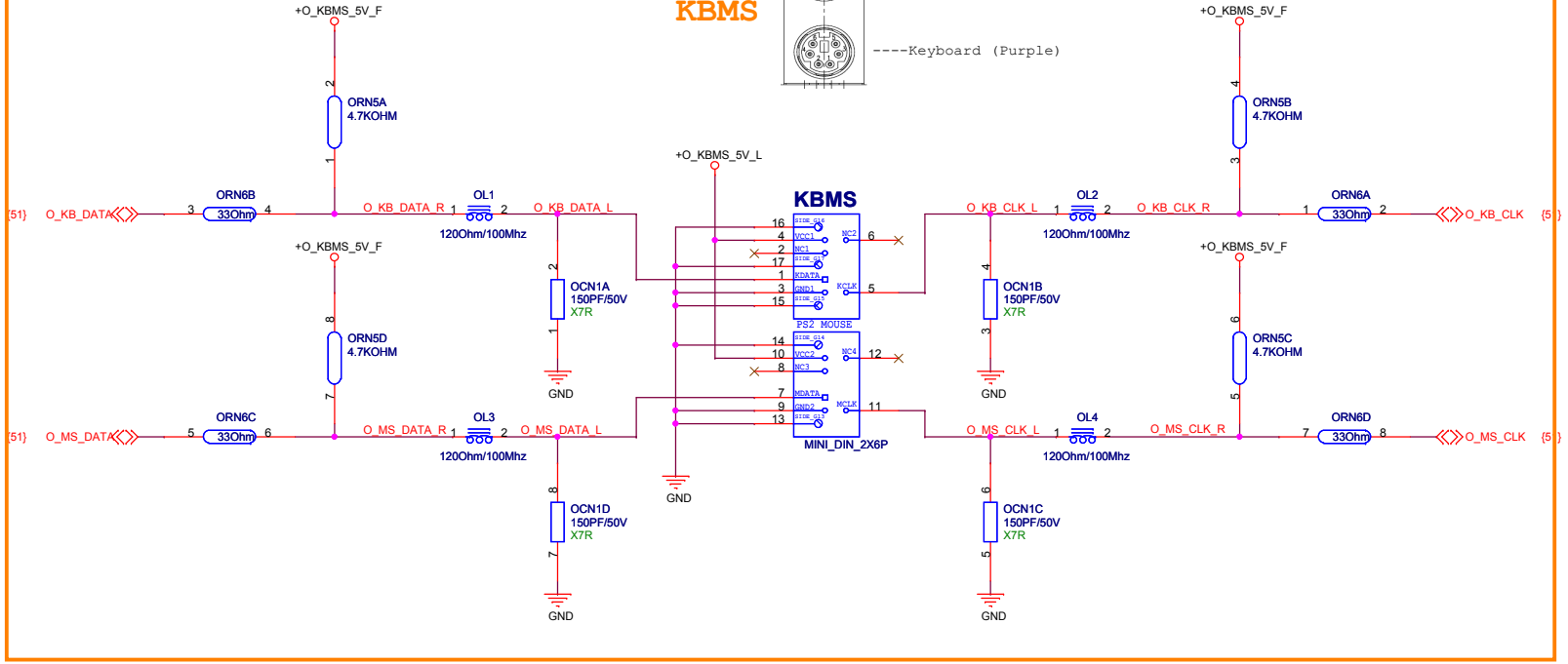
2.Please choose KBPWR (dual power or with jumper)

KBMS

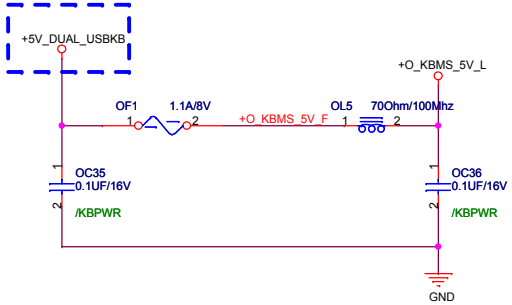


----Mouse (Green)

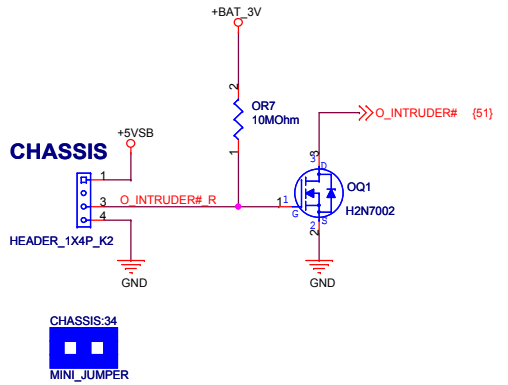
----Keyboard (Purple)



KBPWR(Dual Power)



Intrudor

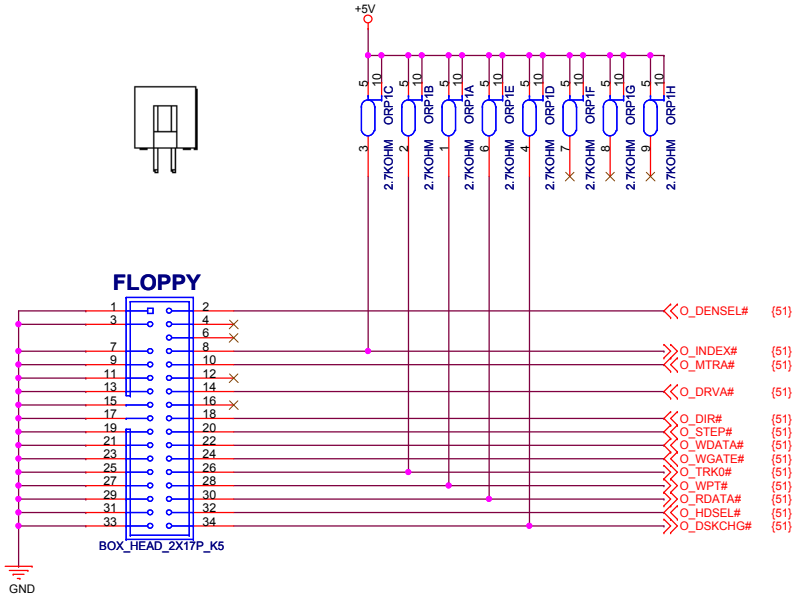


<Variant Name>

ASUSTeK COMPUTER INC	Title: W83627DHG-2(KBMS/USB56)	
	Engineer: C.W. Hunag	
Size: A3	Project Name: P5E-VM DO	Rev: 0.1C
Date: Friday, March 28, 2008	Sheet 52 of 70	

0.1C Beta

Floppy,Standard (Default)



<Variant Name>

ASUSTeK COMPUTER INC

Title :W83627DHG-3(FLOPPY)

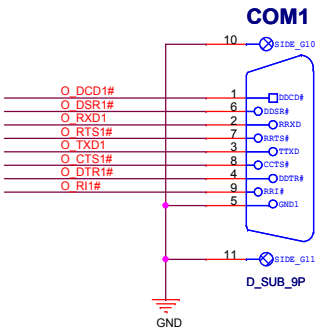
Engineer: C.W. Hunag

Size	Project Name	Rev
A3	P5E-VM DO	0.1C

Date: Friday, March 28, 2008 Sheet 53 of 70

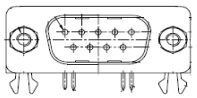
0.1C Beta

COM1
Right Angle (Default)

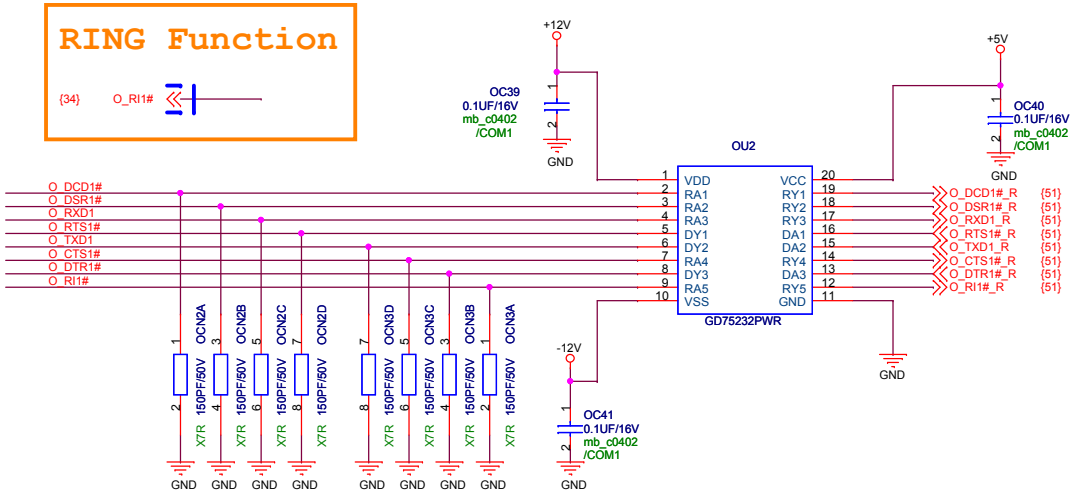


(Green)

(Standard)



RING Function



<Variant Name>

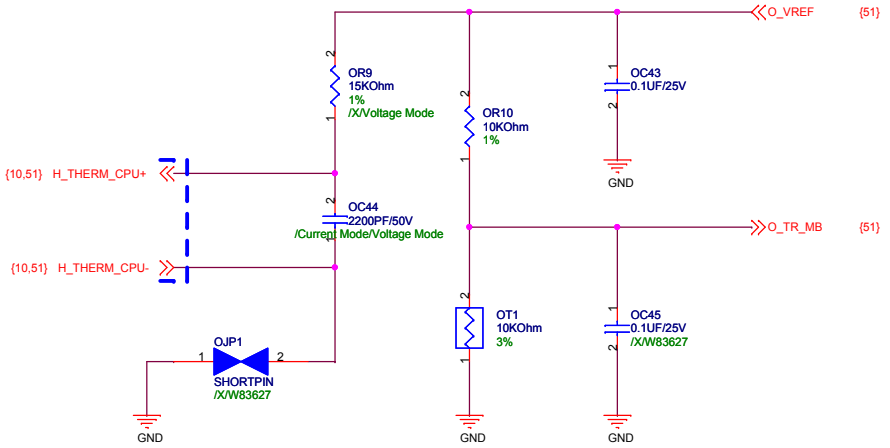
ASUSTeK COMPUTER INC	Title : W83627DHG-4(COM1)	
	Engineer: C.W. Hunag	
Size: A3	Project Name: P5E-VM DO	Rev: 0.1C
Date: Friday, March 28, 2008	Sheet 54 of 70	

0.1C Beta

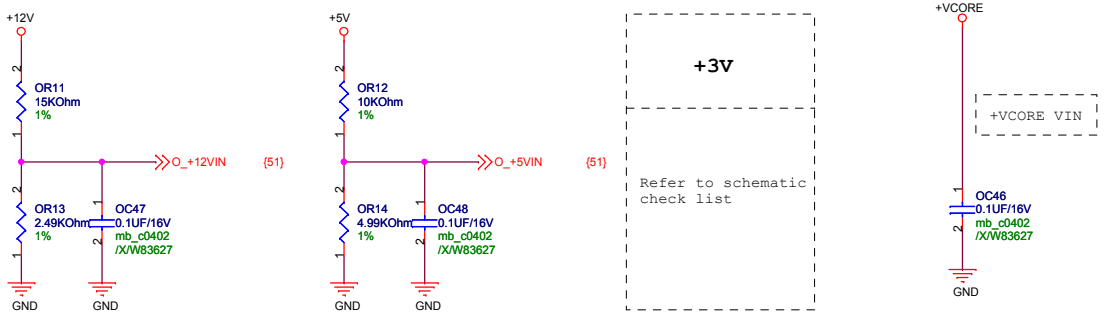
Hardware Monitor for Temperature

BOM Option

	Voltage Mode	Current Mode (Default)
OR9	V	X
OC44	V	V



Hardware Monitor for VIN



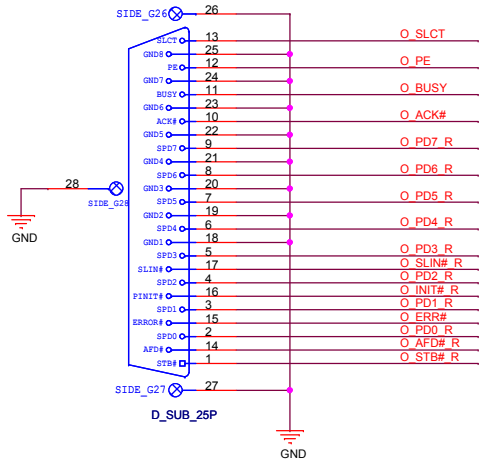
<Variant Name>

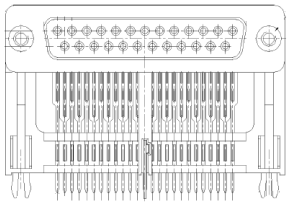
ASUSTeK COMPUTER INC	Title: W83627DHG-6(H/W Monitor)	
	Engineer: C.W. Hunag	
Size: A3	Project Name: P5E-VM DO	Rev: 0.1C
Date: Friday, March 28, 2008	Sheet 55 of 70	

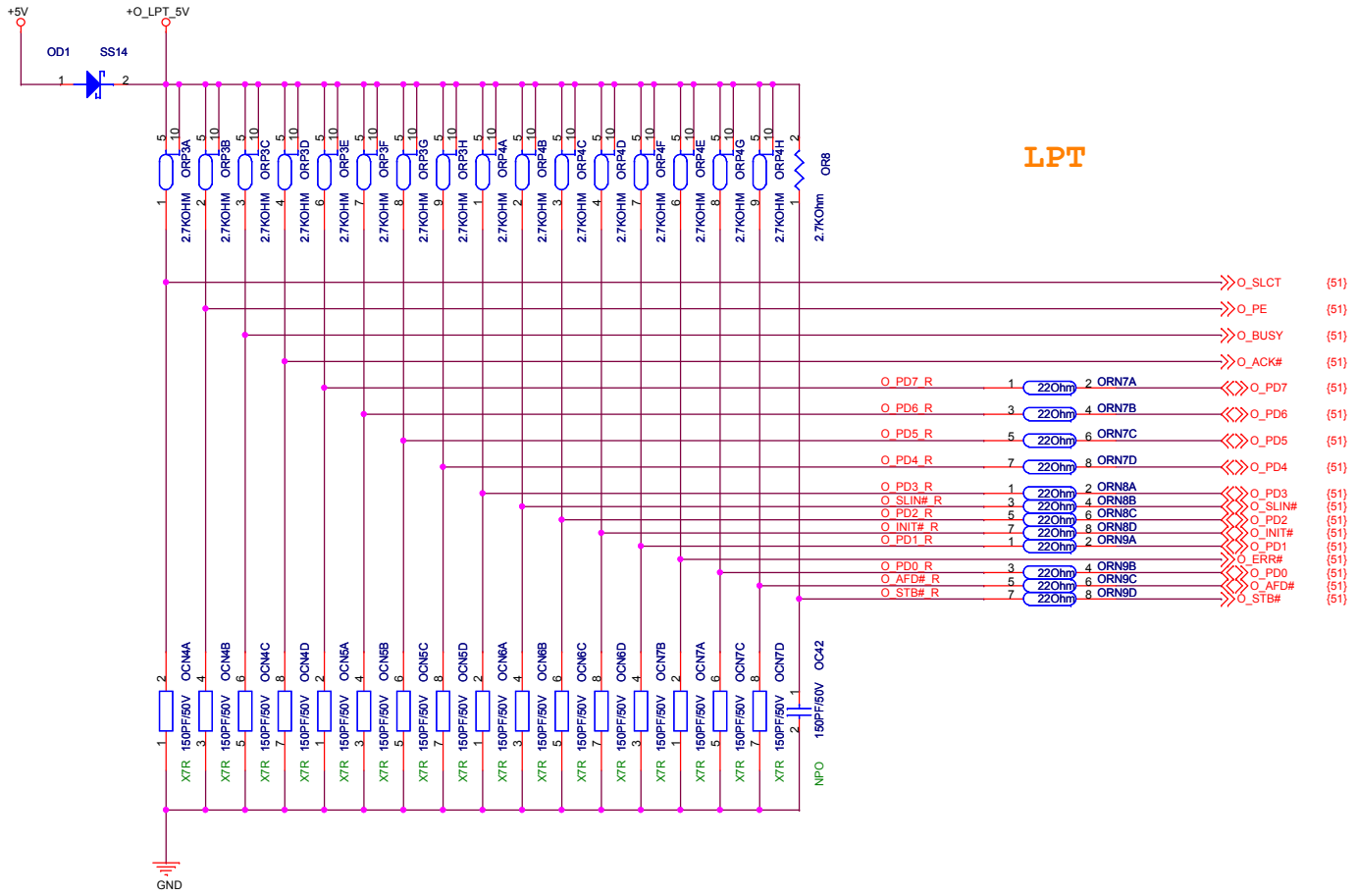
0.1C Beta

D-SUB 25P

LPT



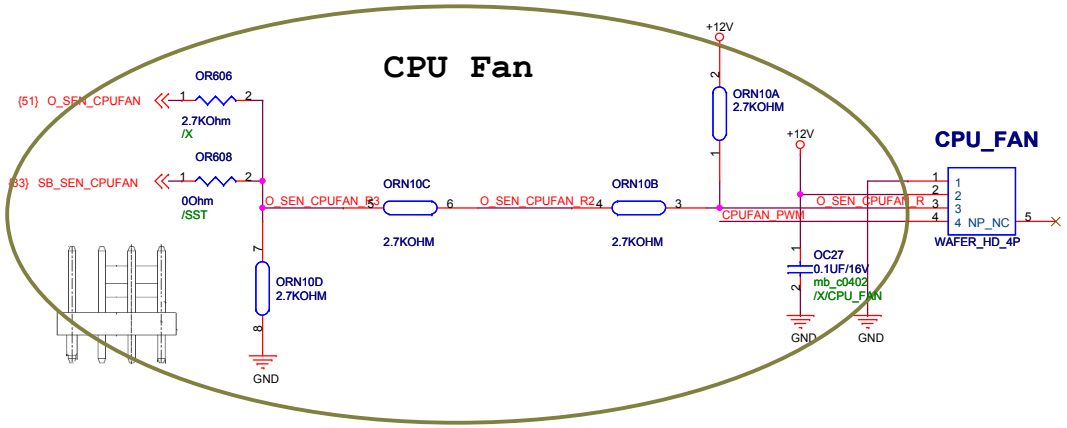


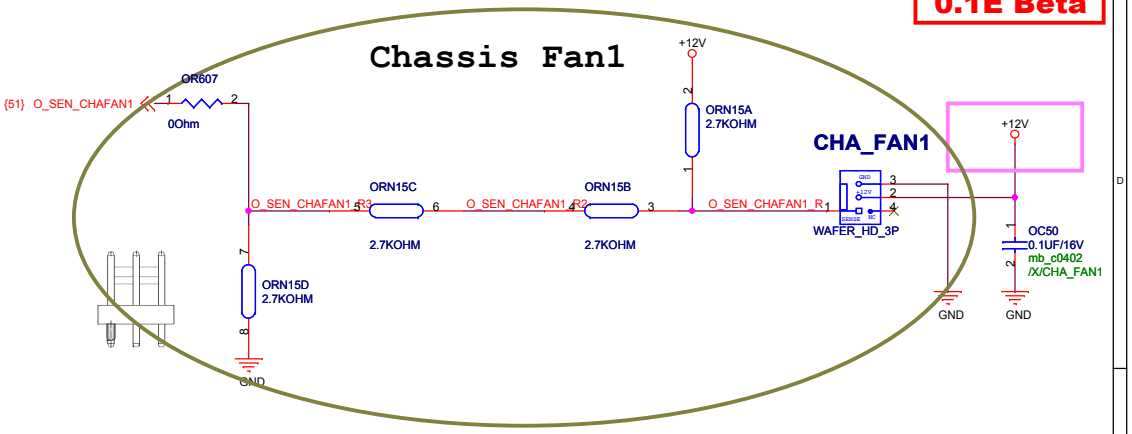


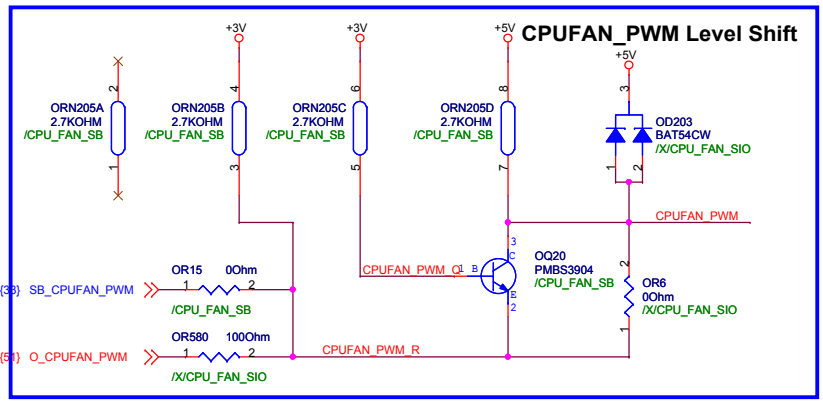
<Variant Name>

ASUSTeK COMPUTER INC	Title : W83627DHG-5(LPT)	
	Engineer: Regin_Chiang	
Size: A3	Project Name: P5E-VM DO	Rev: 1.00
Date: Friday, March 28, 2008	Sheet 56 of 70	

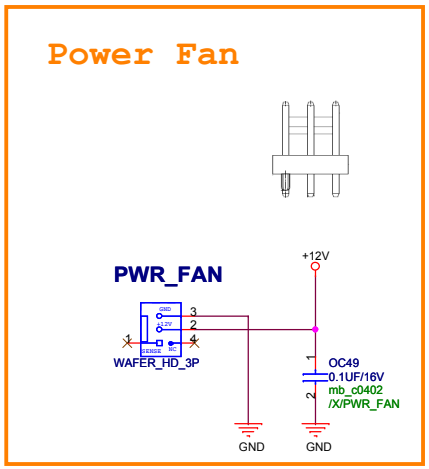
0.1E Beta







DEL
ORN11
20070125



CPU_FAN BOM Option

	SB Control /CPU_FAN_SB	SIO Control /CPU_FAN_SIO
OR580	X	V
OR6	X	V
OD203	X	V
OR15	V	X
ORN205	V	X
OQ20	V	X

<Variant Name>

ASUSTeK COMPUTER INC

Title : W83627DHG-7(FAN/Intrudor)

Engineer: C.W. Hunag

Size	Project Name	Rev
A3	P5E-VM DO	0.1E

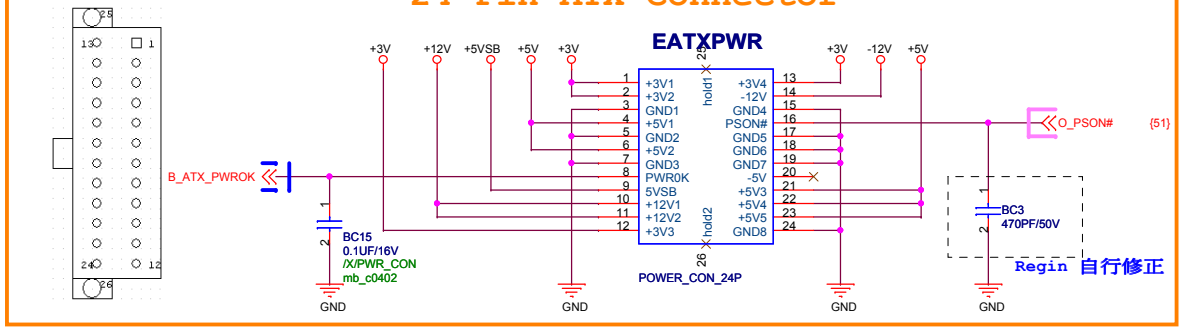
Date: Friday, March 28, 2008 Sheet 57 of 70

0.2A Beta

二選一

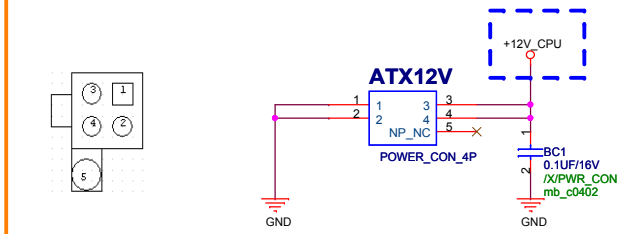
24 Pin ATX Connector

EATXPWR

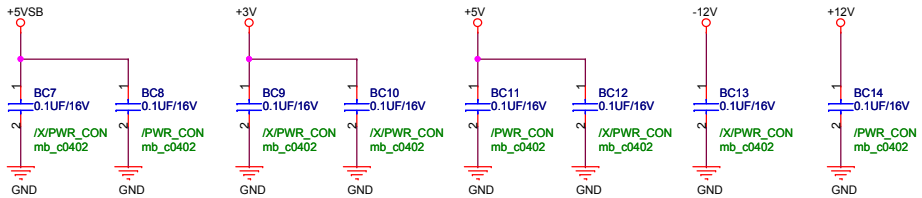


二選一

4 Pin +12V Connector



Bypass/EMI Capacitor



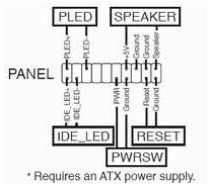
<Variant Name>

ASUS TeK Computer INC	Title : Power Connnecter	
	Engineer: Kenny Chen	
Size: A3	Project Name: P5E-VM DO	Rev: 0.2A
Date: Friday, March 28, 2008	Sheet 58 of 70	

Front Panel

PART Reference 與SIO共用O 並從200編起

Can be del if you don't connect to AUDIO



{4} A_PCBEEP

{34} S_PLED-

+5V

ORN200A 220Ohm

+5VDUAL

ORN200C 220Ohm

R1.01G:Regin
Change ORN200 STD circuit value
from 300 ohm to 220 ohm

PANEL

I_HD_LED-

I_HD_LED+

S_PLED+

S_PLED-

OC205 1000PF/50V /X/PANEL

OC204 1000PF/50V /X/PANEL

OC206 1000PF/50V /X/PANEL

OC207 1000PF/50V /X/PANEL

GND

+3VSB

OR204 8.2KOhm mb_r0402

{51} O_PWRBTN#IN

{7,11,34} O_RSTCON#

O_RSTCON#

HEADER_2X10P

Color:white

A_PCBEEP

BUZZER

2400Hz /X/PANEL

OC200 0.1UF/16V mb_c0402

OC201 0.1UF/16V /X/PANEL mb_c0402

OC203 0.1UF/16V /X/PANEL mb_c0402

OC208 0.1UF/16V /X/PANEL mb_c0402

OR202 33Ohm mb_r0402

A_SPKR_Q

S_SPKR need to check the SB output type of Push-pull or O/D

OR203 2.7KOhm mb_r0402

{34} S_SPKR

S_SPKR_R

OQ200 PMBS3904

Chipset		Action
INTEL	ICH7 ICH8 ICH9	(1)Keep "OR204" (2)The "O_RSTCON#" is connected to SB (3)Delete "O_RSTCON#" off-page net on SIO page
Nvdia	CK804 MCP51	(1)Keep "OR204" (2)The "O_RSTCON#" is connected to SB (3)Delete "O_RSTCON#" off-page net on SIO page (4)Add serial R (22 ohm) on "O_RSTCON#" by AP note for ESD issue.please add R on chipset page.
VIA	VT8237 VT8251	(1)Delete "OR204" (2)The "O_RSTCON#" is connected to SIO (3)Check pull-up resistor & pull-up level on SIO page
SIS	965L	(1)Delete "OR204" (2)The "O_RSTCON#" is connected to SIO (3)Check pull-up resistor & pull-up level on SIO page
ATI	SB600	(1)Delete "OR204" (2)The "O_RSTCON#" is connected to SIO (3)Check pull-up resistor & pull-up level on SIO page

(1)The "O_BTN[1:4]" of GPI need pull-up , Plz check pull-up resistor value & level on SIO or SB page
(2)選擇的GPI 需要是 standby plane , 可以觸發SMI 的GPIO , default 值不限 GPI 或 GPO , 需要在S3,S4,S5 可以維持 GPI state 不會被 reset 或 power OK 被清除

二選一 | 需確認 PES 或與 PM 確認

B

Hot Start

AP_TRIGGER

HEADER_1X2P /X/HOTSTART

O_BTN1 {34}

GND

Standard Circuit

REV. O1_0.2A Beta

0.2A Beta

HD_LED

SB LED

{33} T_SATALED#

{40} I_IDEACTS#

OD201 BAW56W

I_HD_LED-

Change the net name to combine the HD LED active

請按照下列 Net name 修改: I_IDEACTP# → II_IDEACTP#
I_IDEACTS# → II_IDEACTS#
T1_SATALED# → T2_SATALED#

用不到的 net 請Delete,並打x

R1.01G:Regin
Change ORN200 STD circuit value
from 300 ohm to 220 ohm

Standby LED

+5VSB

ORN200D 220Ohm

ORN200B 220Ohm

O_SBLED_PWR

SB_PWR

GREEN

GND

<Variant Name>

Title : Panel&HotStart

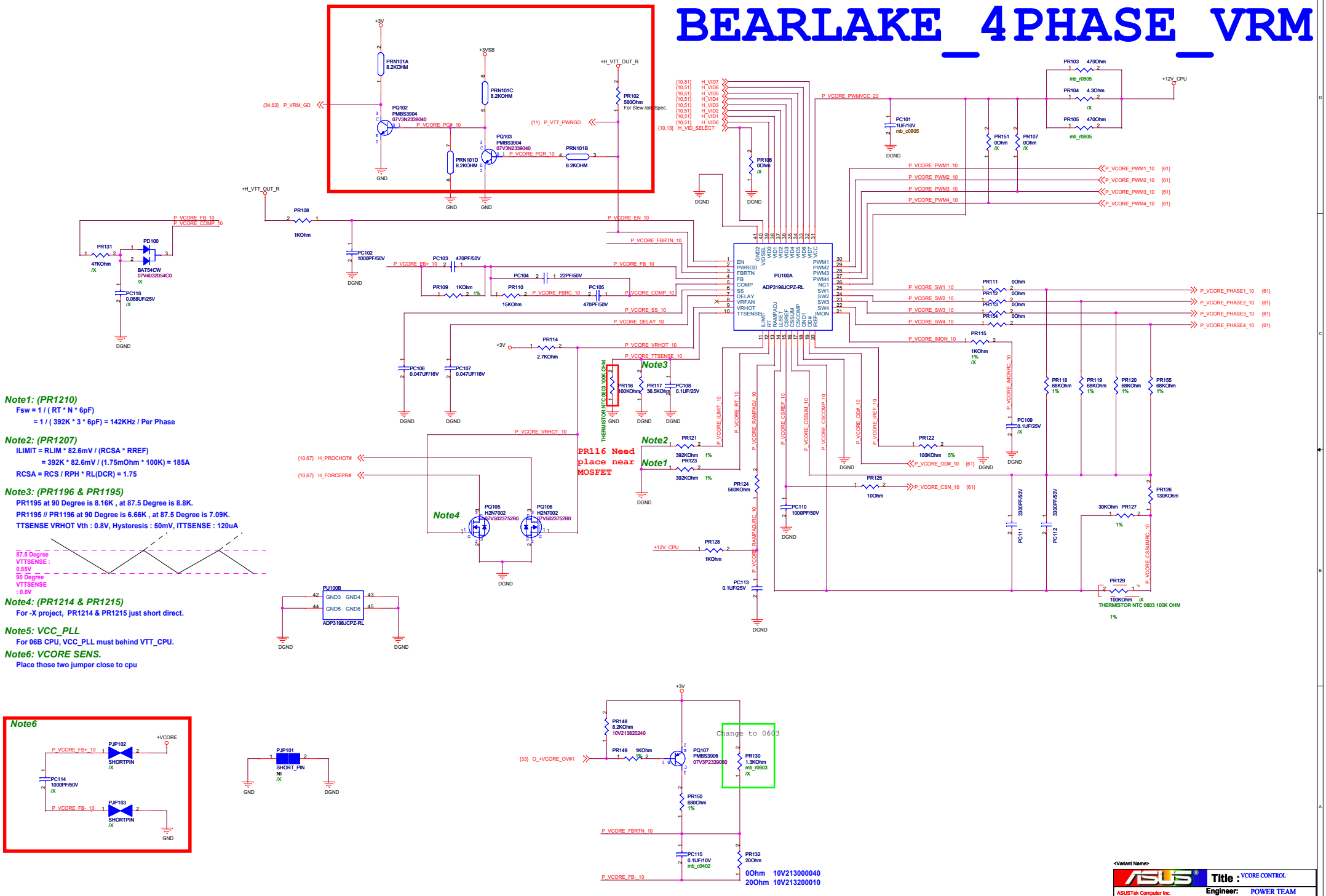
ASUS TeK Computer INC

Engineer: Kenny Chen

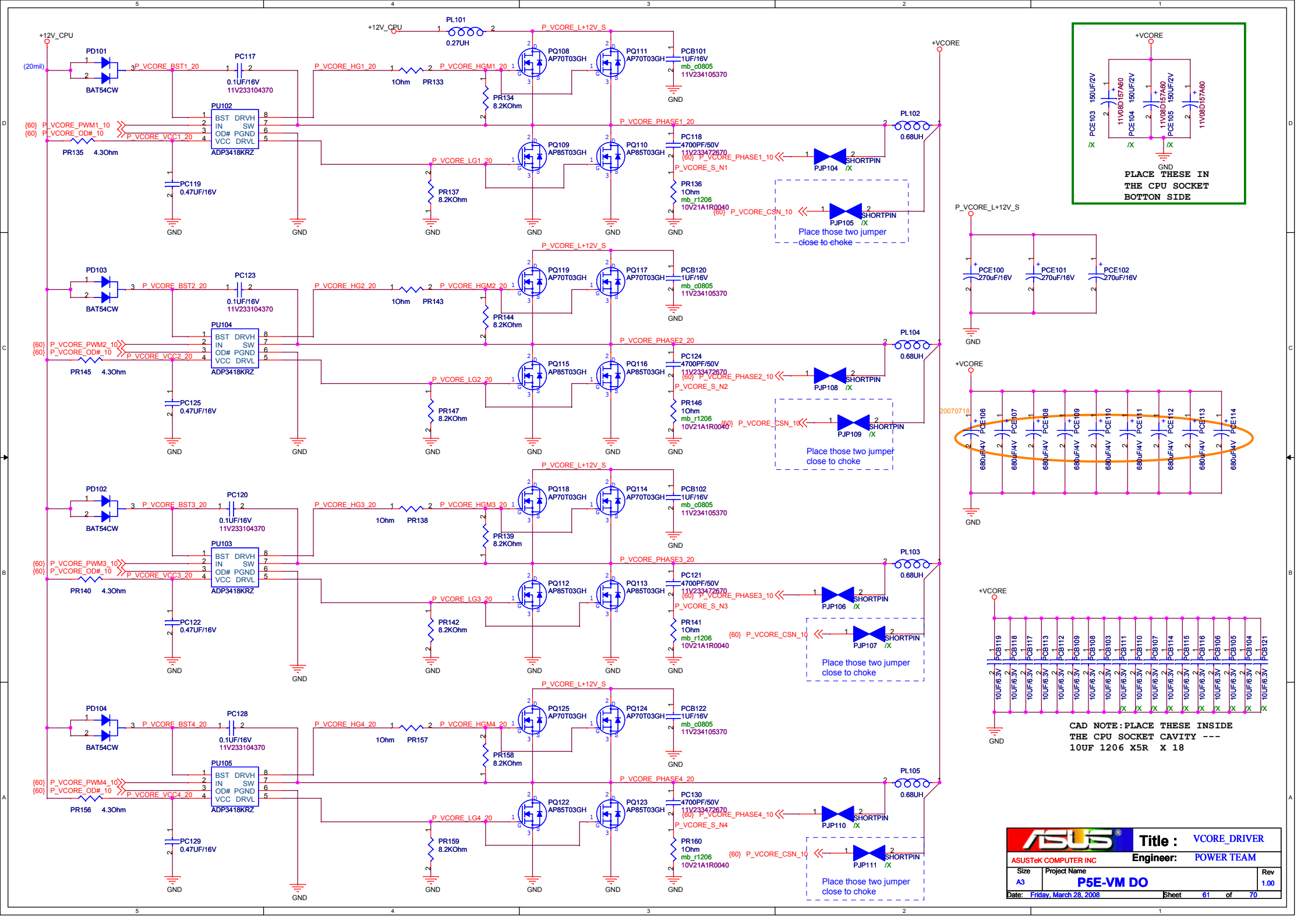
Size	Project Name	Rev
A3	P5E-VM DO	0.2A

Date: Friday, March 28, 2008 Sheet 59 of 70

BEARLAKE_4PHASE_VRM

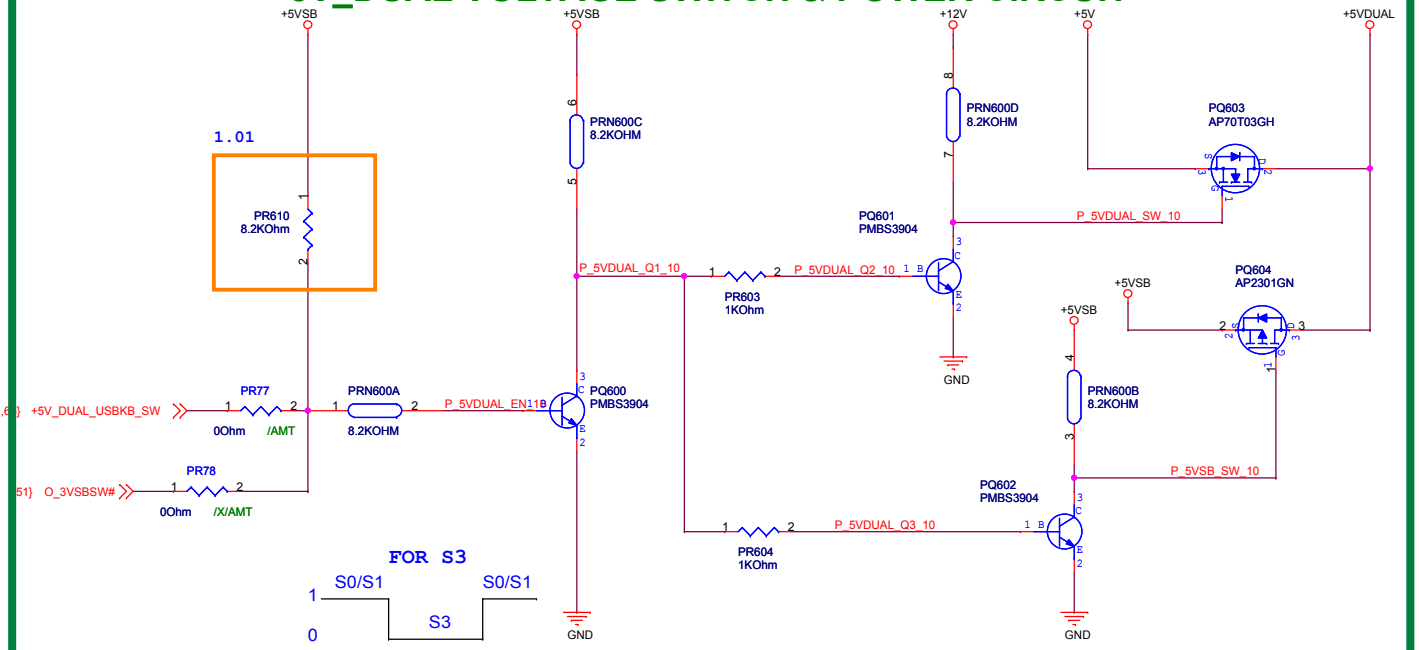


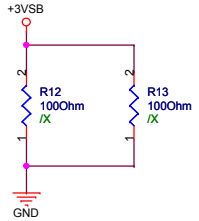
<Variant Name>
ASUSTek Computer Inc.
Title : VCORE CONTROL
Engineer: POWER TEAM
Size A2
Project Name P5E-VM DO
Rev 1.00
Date: Friday, March 28, 2008
Sheet 60 of 70



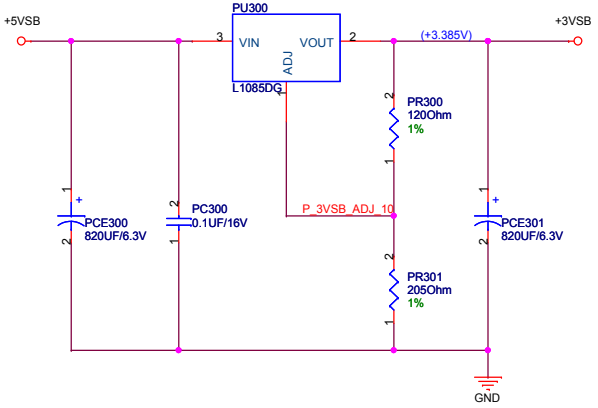
ASUSTeK COMPUTER INC	Title :	VCORE_DRIVER
	Engineer:	POWER TEAM
Size: A3	Project Name: P5E-VM DO	Rev: 1.00
Date: Friday, March 28, 2008	Sheet 61 of 70	

+5V_DUAL VOLTAGE SWITCH & POWER CIRCUIT

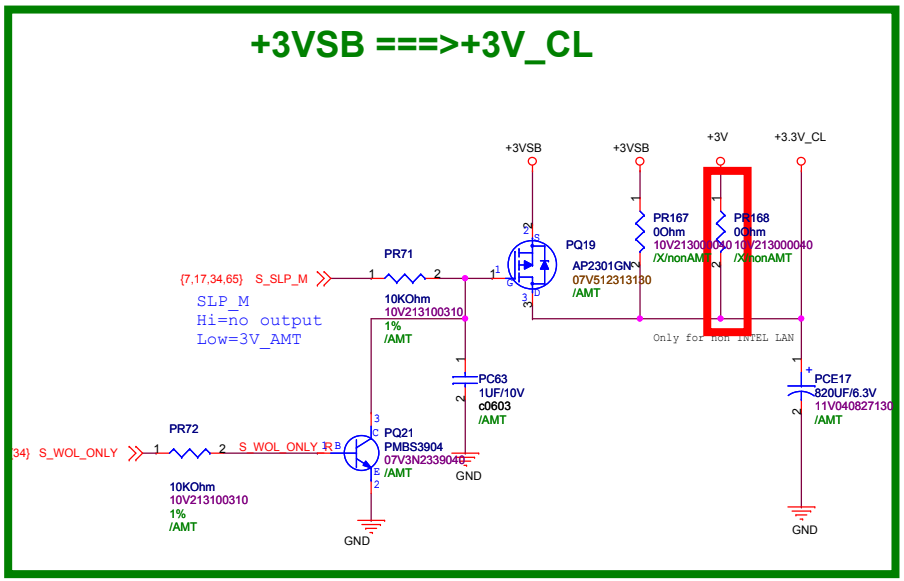




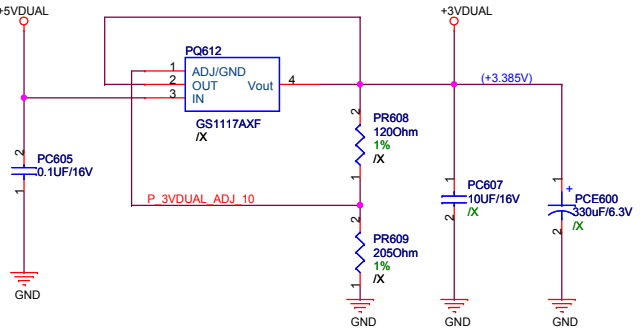
+5VSB ====>+3VSB Io: 2A



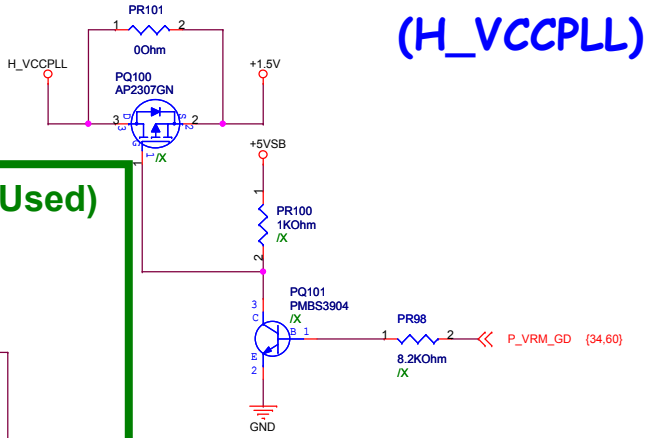
+3VSB ===>+3V_CL



+5VDUAL==>+3VDUAL(Clock Gen Used)



(H_VCCPLL)

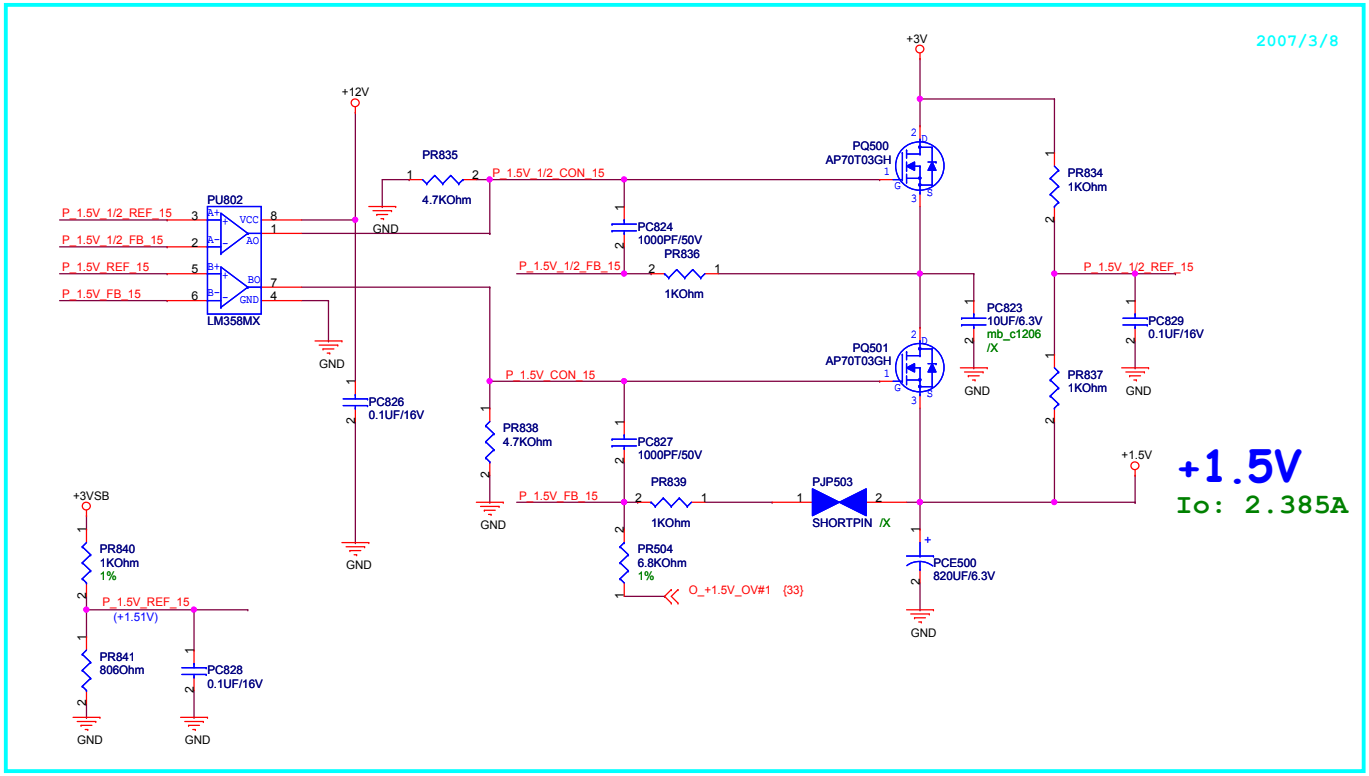


<Variant Name>

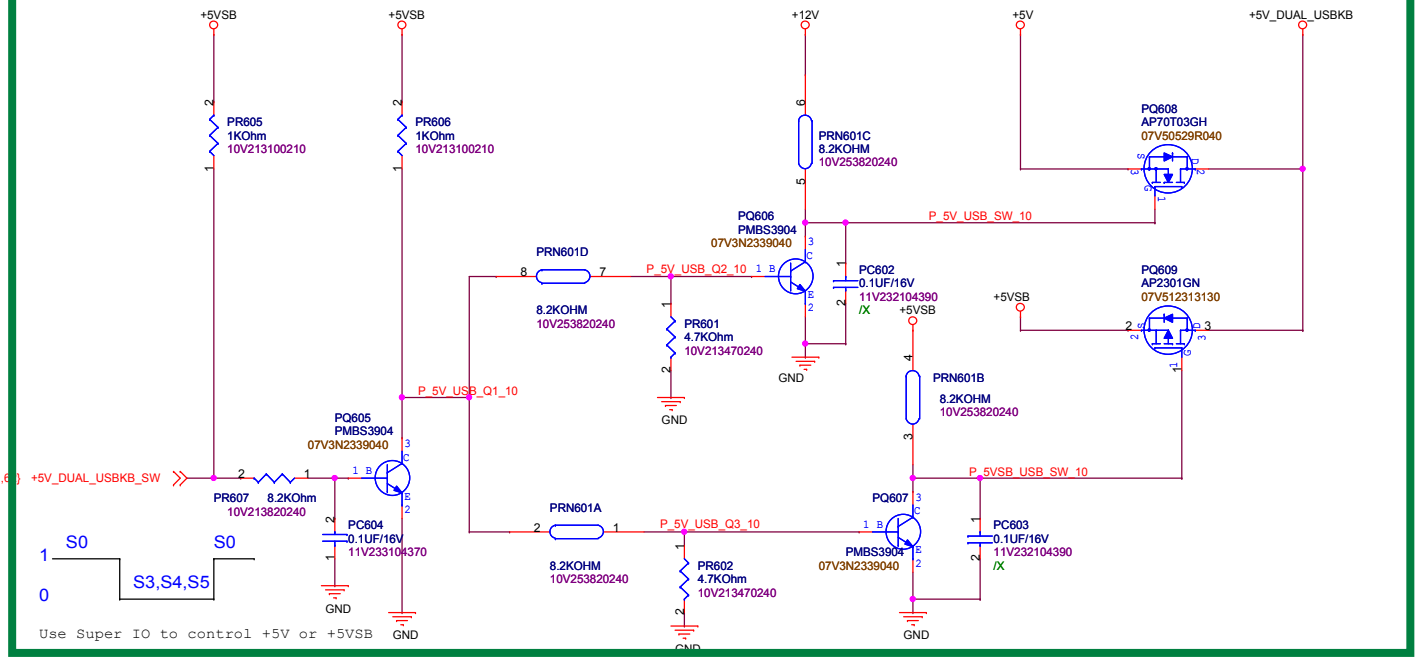
+5V_DUAL&+3VSB&+3V_DUAL

ASUSTeK COMPUTER INC	Title :	
	Engineer:	
Size: A3	Project Name: P5E-VM DO	Rev: 1.00G
Date: Friday, March 28, 2008	Sheet 62 of 70	

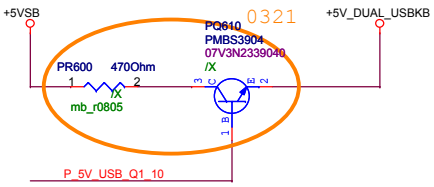
OV1#	+1.5V
X	+1.510V
L	+1.732V



+5VSB_USBKB VOLTAGE & POWER CIRCUIT



+5VDUAL_USBKB UVP CIRCUIT



<Variant Name>

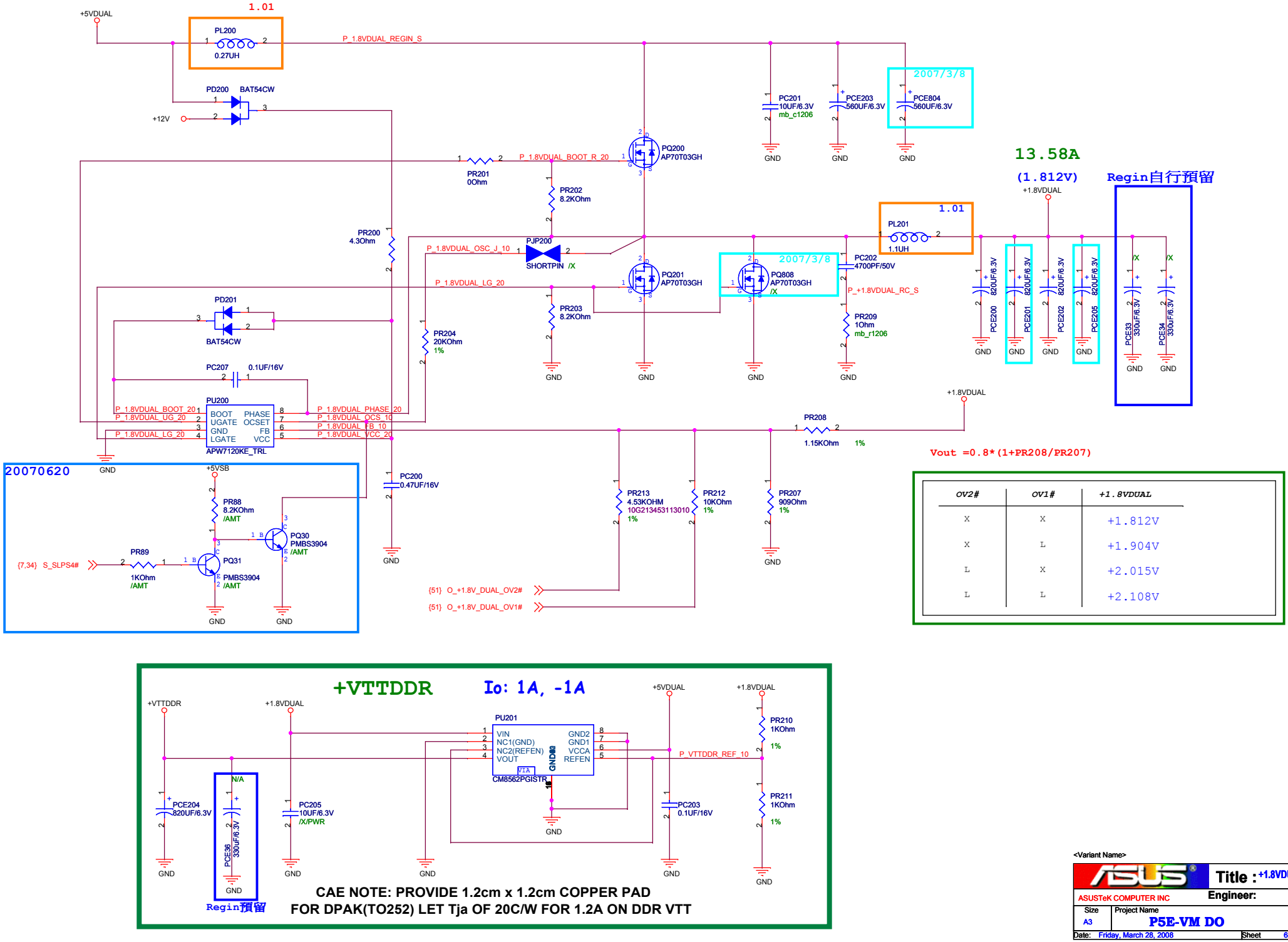
ASUSTeK COMPUTER INC

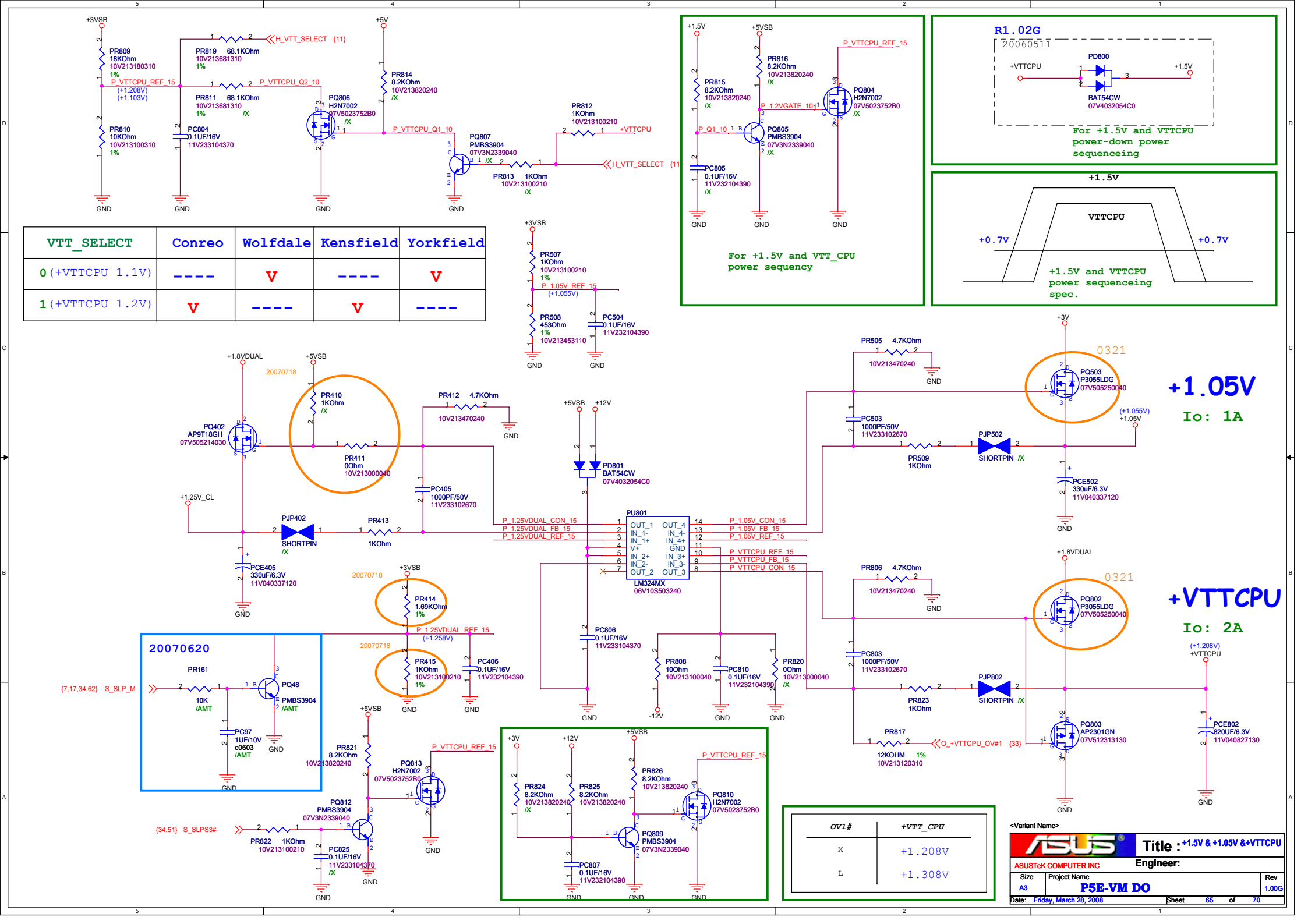
Title : +1.5V

Engineer:

Size	Project Name	Rev
A3	P5E-VM DO	1.00G

Date: Friday, March 28, 2008 Sheet 63 of 70


+5VDUAL
1.01
PL200
0.27UH
P_1.8VDUAL_REGIN_S
PD200 BAT54CW
+12V
PC201
10UF/6.3V
mb_c1206
PCE203
560UF/6.3V
2007/3/8
PCE804
560UF/6.3V
GND
PQ200
AP70T03GH
PR201
0Ohm
P_1.8VDUAL_BOOT_R_20
PR202
8.2KOhm
PR200
4.3Ohm
PJP200
SHORTPIN /X
P_1.8VDUAL_OSC_J_10
PQ201
AP70T03GH
PQ808
AP70T03GH
/X
PC202
4700PF/50V
P_+1.8VDUAL_RC_S
PR209
1Ohm
mb_r1206
PL201
1.1UH
13.58A
(1.812V)
Regin自行預留
+1.8VDUAL
PCE200
PCE201
PCE202
PCE205
820UF/6.3V
PCE33
PCE34
330uF/6.3V
PD201
BAT54CW
P_1.8VDUAL_LG_20
PR203
8.2KOhm
PR204
20KOhm
1%
PC207
0.1UF/16V
PU200
BOOT
UGATE
GND
LGATE
PHASE
OCSET
FB
VCC
APW7120KE_TRL
P_1.8VDUAL_BOOT_20
P_1.8VDUAL_UG_20
P_1.8VDUAL_LG_20
P_1.8VDUAL_PHASE_20
P_1.8VDUAL_OCS_10
P_1.8VDUAL_FB_10
P_1.8VDUAL_VCC_20
PR208
1.15KOhm
1%
Vout =0.8*(1+PR208/PR207)
20070620
+5VSB
PR88
8.2KOhm
/AMT
PQ30
PMBS3904
/AMT
PR89
1KOhm
/AMT
PQ31
PMBS3904
/AMT
{7,34} S_SLPS4#
PC200
0.47UF/16V
PR213
4.53KOHM
10G2134531130 10
PR212
10KOhm
PR207
909Ohm
{51} O_+1.8V_DUAL_OV2#
{51} O_+1.8V_DUAL_OV1#
OV2#
OV1#
+1.8VDUAL
X X +1.812V
X L +1.904V
L X +2.015V
L L +2.108V
+VTTDDR
Io: 1A, -1A
+VTTDDR
+1.8VDUAL
+5VDUAL
PU201
VIN
NC1(GND)
NC2(REFEN)
VOUT
GND2
GND1
VCCA
REFEN
GNDa
VIA
CM8562PGISTR
P_VTTDDR_REF_10
PR210
1KOhm
1%
PR211
1KOhm
1%
PC203
0.1UF/16V
PCE204
820UF/6.3V
N/A
PCE36
330uF/6.3V
PC205
10UF/6.3V
/X/PWR
Regin預留
CAE NOTE: PROVIDE 1.2cm x 1.2cm COPPER PAD
FOR DPAK(TO252) LET Tja OF 20C/W FOR 1.2A ON DDR VTT
<Variant Name>
Title : +1.8VDUAL & +VTTDDR
ASUSTeK COMPUTER INC
Engineer:
Size A3
Project Name P5E-VM DO
Rev 1.00G
Date: Friday, March 28, 2008
Sheet 64 of 70



VTT_SELECT	Conreo	Wolfdale	Kensfield	Yorkfield
0 (+VTTCPU 1.1V)	----	V	----	V
1 (+VTTCPU 1.2V)	V	----	V	----

OV1#	+VTT_CPU
X	+1.208V
L	+1.308V

<Variant Name>

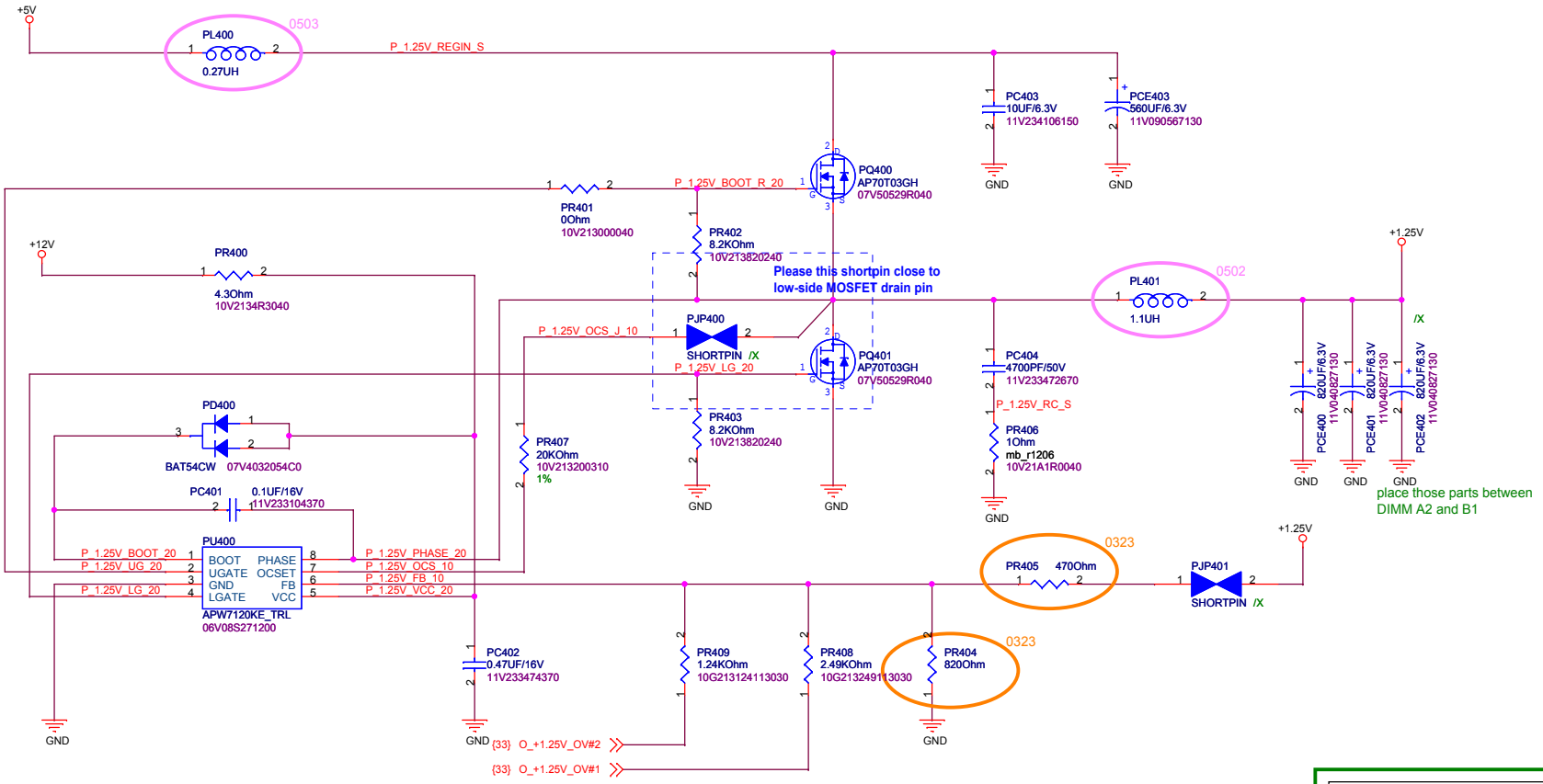
ASUSTeK COMPUTER INC

Title : +1.5V & +1.05V &+VTTCPU

Engineer:

Size	Project Name	Rev
A3	P5E-VM DO	1.00G

Date: Friday, March 28, 2008 Sheet 65 of 70



OV2#	OV1#	+1.25V	
X	X	+1.250V	(+1.258V)
X	L	+1.400V	(+1.410V)
L	X	+1.550V	(+1.562V)
L	L	+1.700V	(+1.714V)

<Variant Name>

ASUSTeK COMPUTER INC

Title : +1.25V

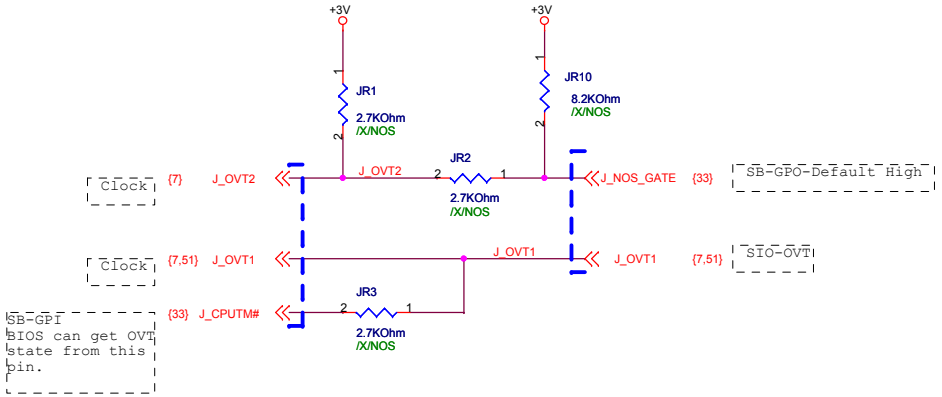
Engineer:

Size	Project Name	Rev
A3	P5E-VM DO	1.00G

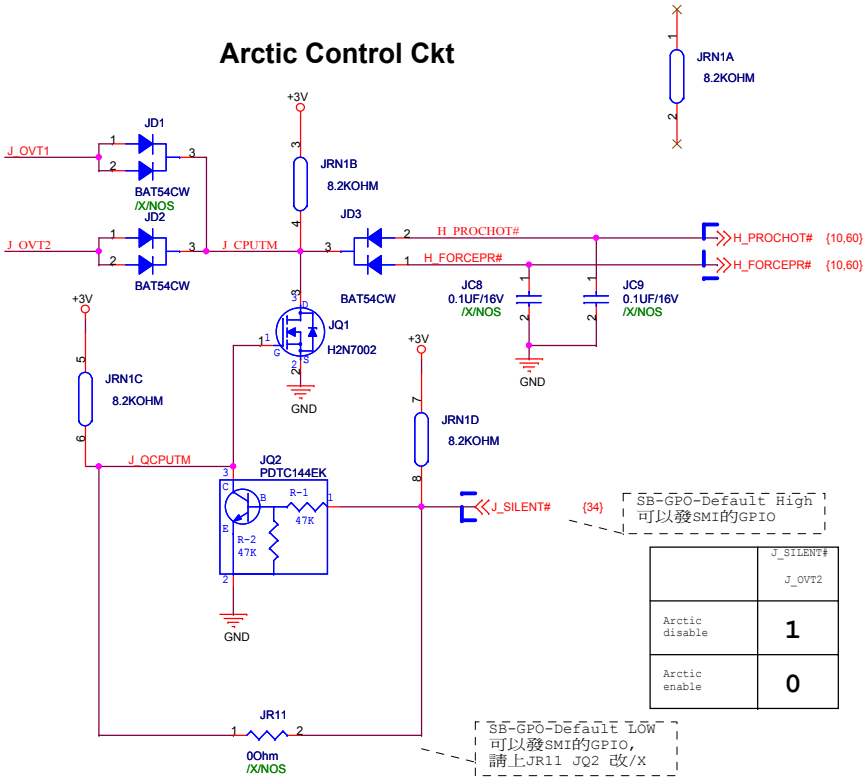
Date: Friday, March 28, 2008 Sheet 66 of 70

NOS Control Ckt

	J_OVT1	J_OVT2 NOS_GATE
NOS disable	Don't Care	1
NOS enable heavy loading	0	0
NOS enable normal loading	1	0



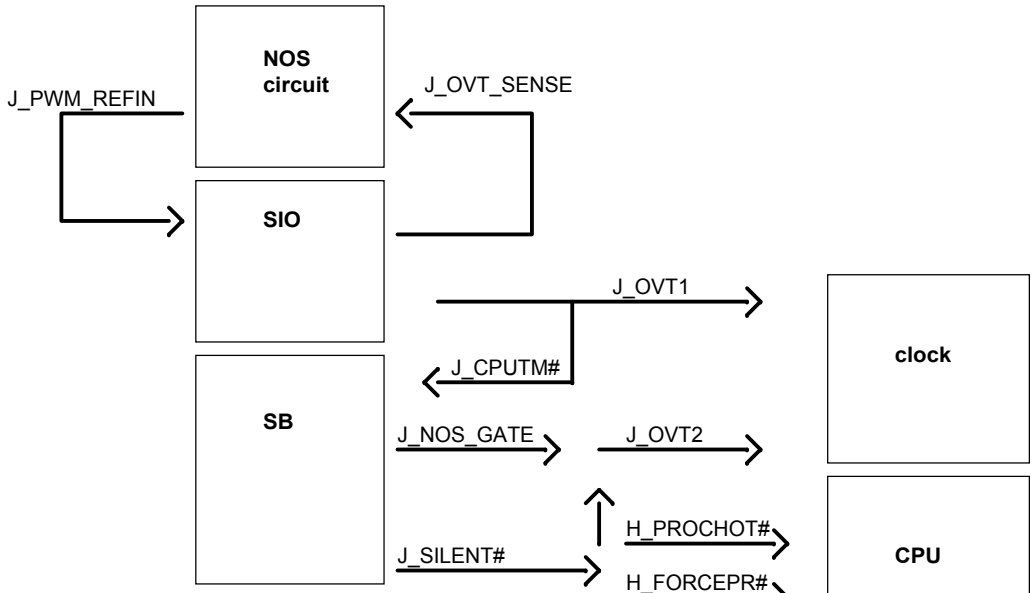
Arctic Control Ckt



	J_SILENT# J_OVT2
Arctic disable	1
Arctic enable	0

	J_SILENT# J_OVT2
Arctic disable	0
Arctic enable	1

Function Block :



Standard Circuit	
NOS	Intel
REV.	J_0.1B beta

LOGO_STD_NOS
/X/NOS

<Variant Name>

ASUSTek Computer Inc.

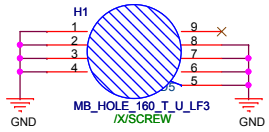
Title : NOS(intel)

Engineer: Makishin_Huang

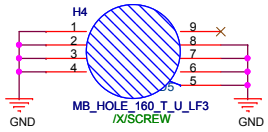
Size	Project Name	Rev
A3	P5E-VM DO	0.1B

Date: Friday, March 28, 2008 Sheet 67 of 70

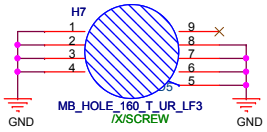
0.1B Beta



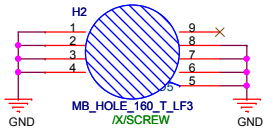
origin-xy:(1300.00, 9350.00)



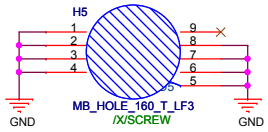
origin-xy:(6500.00, 9350.00)



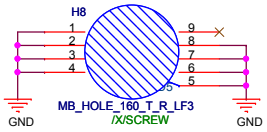
origin-xy:(9350.00, 9350.00)



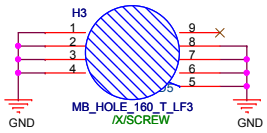
origin-xy:(400.00, 3150.00)



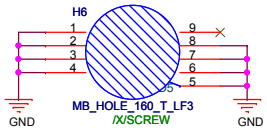
origin-xy:(6500.00, 3150.00)



origin-xy:(9350.00, 3150.00)



origin-xy:(400.00, 1350.00)



origin-xy:(6500.00, 550.00)

9.6 inch

(X,Y)=(0,0)

<9.6 inch

9.6 inch

Screw Select

	Standard (9.6 x 9.6)	scale down (9.6 x <9.6)
H1	V	V
H2	V	V
H3	V	V
H4	V	V
H5	V	V
H6	V	V
H7	V	X
H8	V	X

MB SCREW FOOTPRINT

MB_HOLE_160_T_LF3

MB_HOLE_160_T_U_LF3

MB_HOLE_160_T_R_LF3

MB_HOLE_160_T_UR_LF3

<Variant Name>

Title : uATX Sreial Screw Hole

ASUS TeK Computer INC

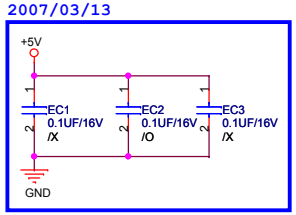
Engineer: Kenny Chen

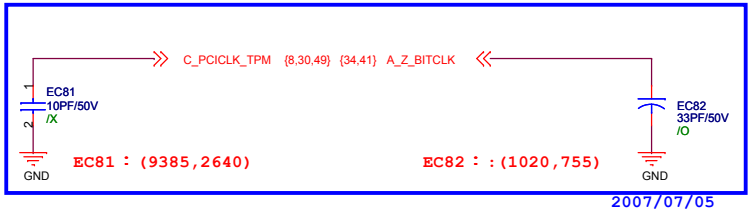
Size	Project Name	Rev
A3	P5E-VM DO	0.1B

Date: Friday, March 28, 2008 Sheet 68 of 70

2007/07/06

JMB368 FAE Suggestion
2007/03/13

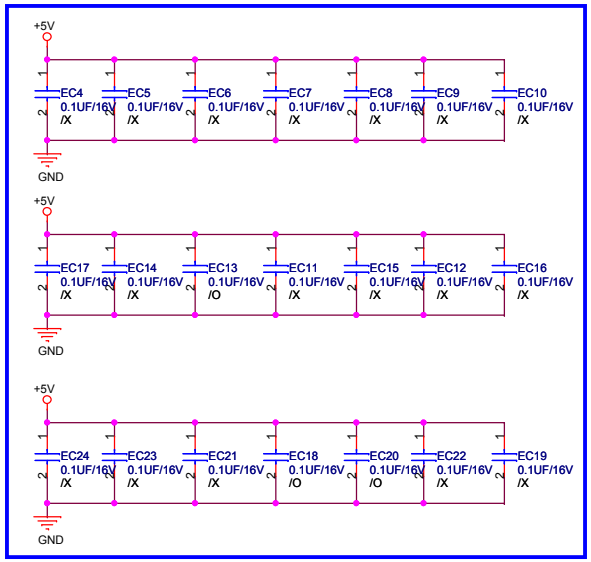




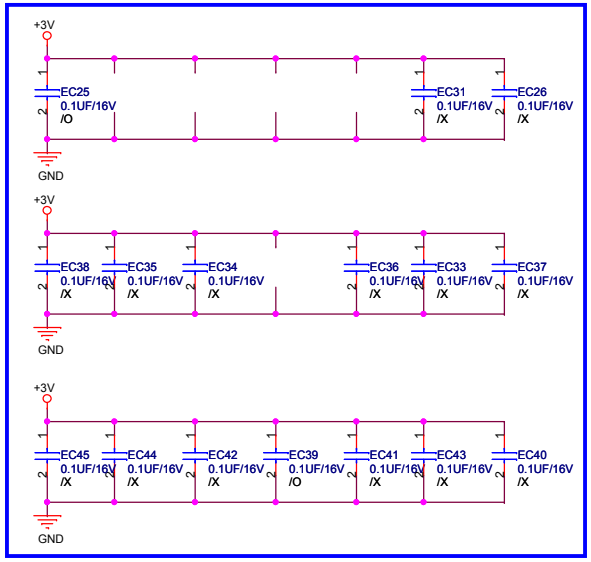
EC81 : (9385,2640)

EC82 : :(1020,755)

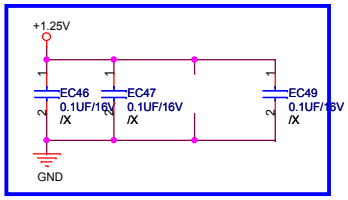
EC4~EC24 For EMI Used



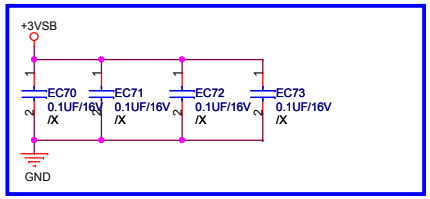
EC25~EC45 For EMI Used



EC46~EC49 For EMI Used



2007/07/05



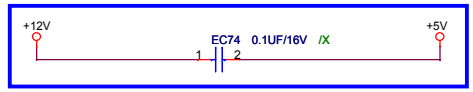
EC70 : (8365,9140)

EC71 : (9110,2890)

EC72 : (7240,925)

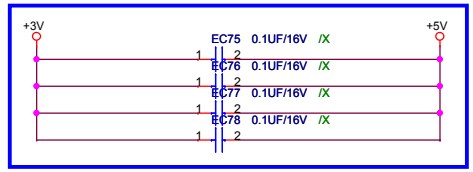
EC73 : (5470,1655)

2007/07/05



EC74 : (1370,3075)

2007/07/05



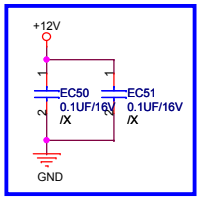
EC75 : (1740,3420)

EC76 : (3205,635)

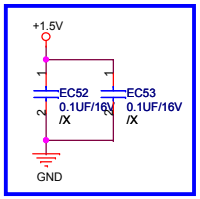
EC77 : (4610,2145)

EC78 : (8120,835)

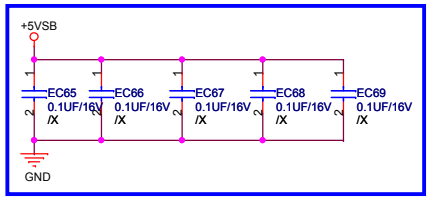
EC50~EC51 For EMI Used



EC52~EC53 For EMI Used



2007/07/05



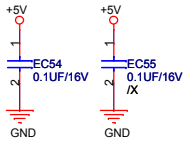
EC65 : (2605,5830)

EC66 : (1675,180)

EC67 : (2870,285)

EC68 : (5950,190)

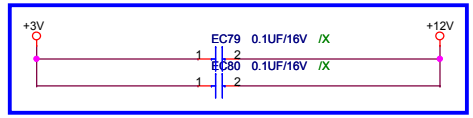
EC69 : (9415,2915)



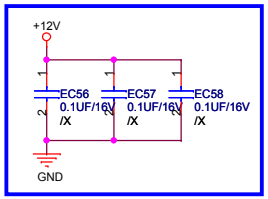
2007/07/05

EC79 : (2020,2835)

EC80 : (8190,3760)



2007/07/05

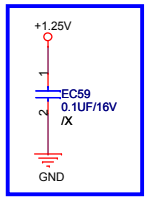


EC56 : (7075,2870)

EC57 : (4825,2200)

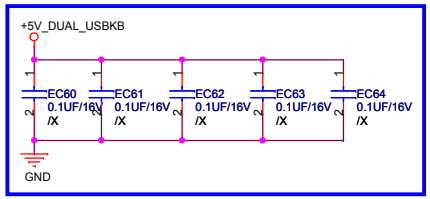
EC58 : (1140,6385)

2007/07/05



EC59 : (4300,3515)

2007/07/05



EC60 : (1370,5355)

EC61 : (1300,4755)

EC62 : (1855,425)

EC63 : (5855,465)

EC64 : (8505,420)

<Variant Name>

<OrgName>

Title : EMI CAP

Engineer: <OrgAddr1>

Size	Project Name	Rev
A3	P5E-VM DO	1.00G

Date: Friday, March 28, 2008 Sheet 69 of 70

PCB Rev	Change List
R1.00G	Initial Version
R1.01G	1. Swap SATA 3 & SATA 4 To support ICH9 Base version Chipset 2. Update Core team ASM4131 Standard circuit 3. Unify the Power Solution Choke for Channel request
R1.02G	1.Modify the SATA 3 port one set differential signals (Page 35) 2.Change VRN104 instead of VR40 & VR41 in order to reduce high speed differential sginal stub effect (Page 24) 3.Add OR611 to reserve SIO PWROK issue to pull-up +3VSB(Page 53) 4. For All Channel Request to change Power Choke pitch size on PL102,PL103,PL104,PL201

<Variant Name>

ASUSTeK COMPUTER INC

Title : Change List

Engineer: Regin_Chiang

Size	Project Name	Rev
A3	P5E-VM DO	1.00

Date: Friday, March 28, 2008 Sheet 70 of 70